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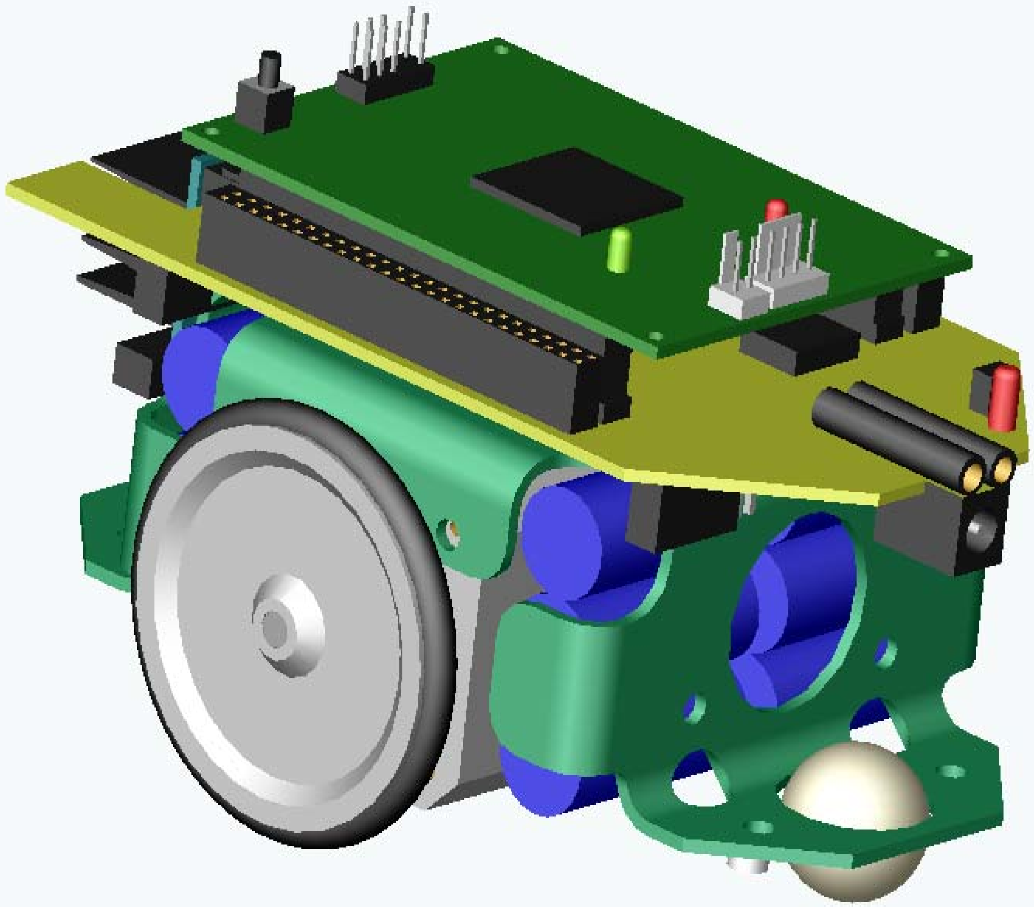
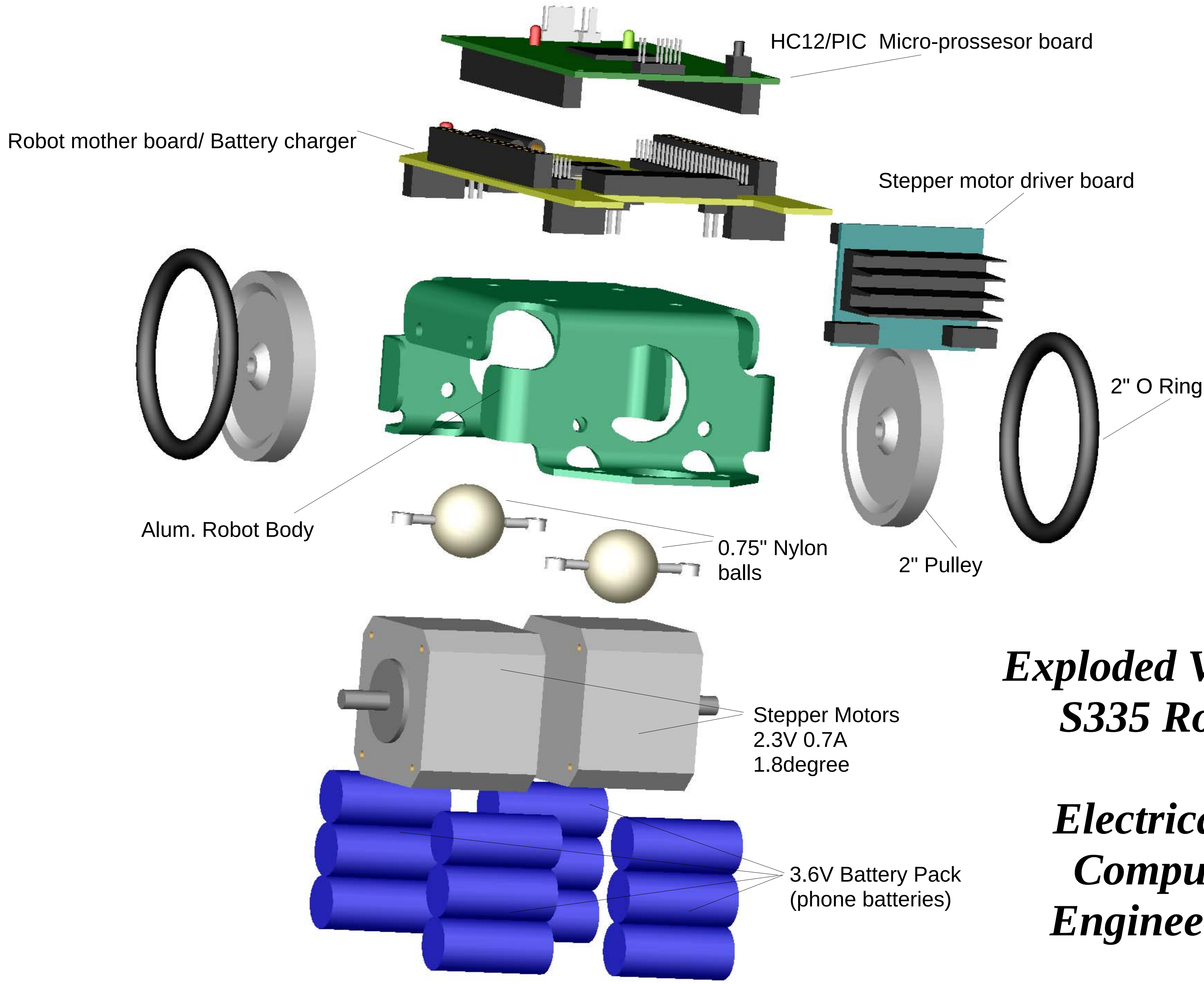


S335



Exploded View of S335 Robot

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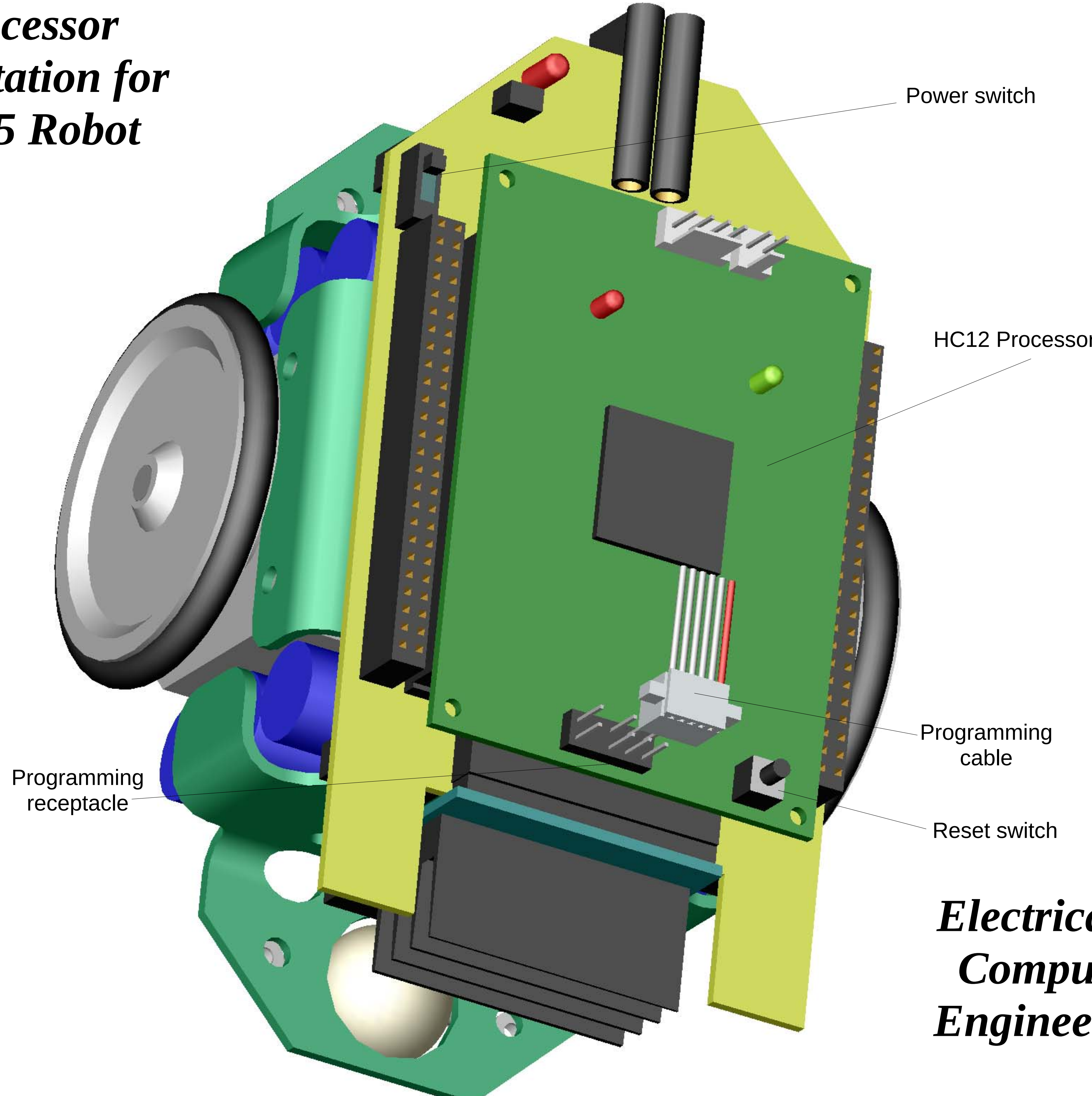
Processor Orientation for S335 Robot



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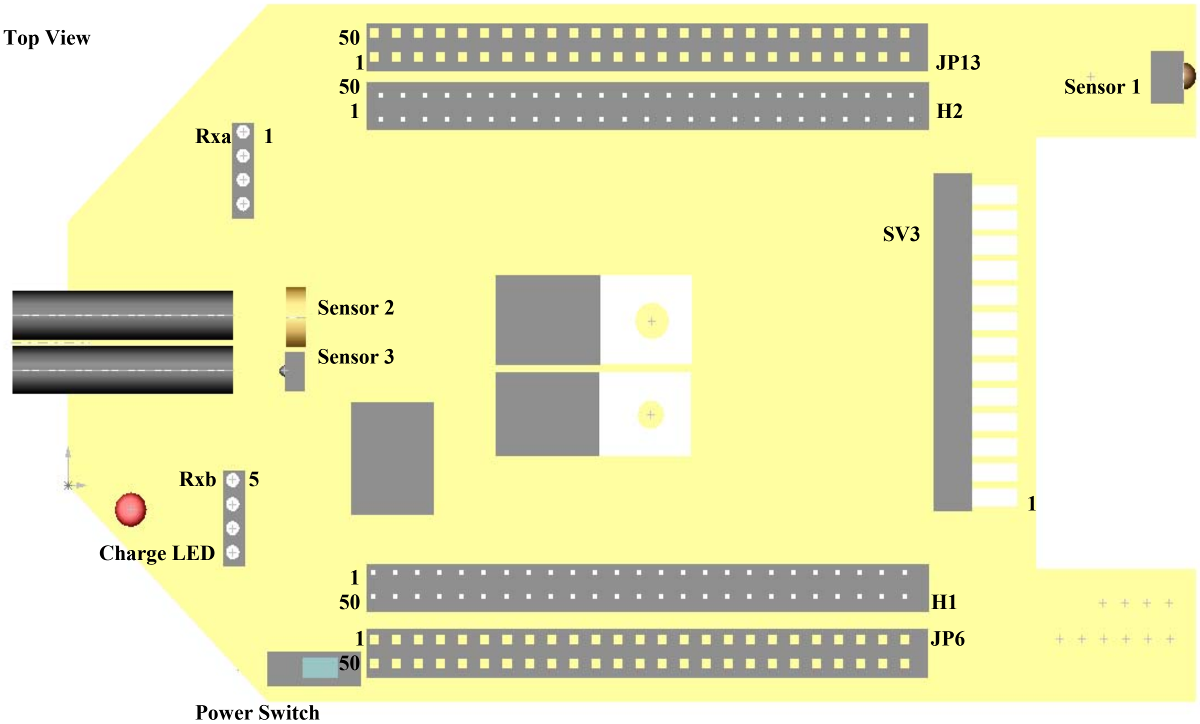
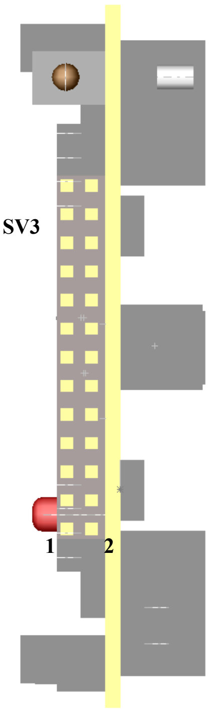




Side View(from Back)

JP6 – Port Header

6	HC12	PIC	#	HC12	PIC
50	Gnd	Gnd	1	PS4	NC
49	Gnd	Gnd	2	PS5	NC
48	PS0	RC4	3	PS6	RC3
47	+5V	+5V	4	PT7	RC1/RB3
46	PE1	RB0	5	PS1	RC5
45	PE0	NC	6	PT7	RC1/RB3
44	Reset	Reset	7	PT6	RC2
43	PE7	NC	8	PT5	RB7
42	PH0	RB0	9	PT4	RB6
41	PH1	RB1	10	PT3	RB5
40	PH2	RB2	11	PT2	RB4
39	PH3	RB3	12	PT1	RC0
38	PH4	RB4	13	PT0	RA4
37	PH5	RB5	14	PP7	RA5
36	PH6	RB6	15	PP6	RA4
35	PH7	RB7	16	PP5	RA3
34	PS2	RC7	17	PP4	RA2
33	PE4	RE2	18	PP3	RA1
32	PS3	RC6	19	PP2	RC1/RB3
31	VRL	NC	20	PP1	RC2
30	VHL	NC	21	PP0	RA0
29	PAD04	AN4 (RA5)	22	PAD00	AN0 (RA0)
28	PAD05	AN5 (RE0)	23	PAD01	AN1 (RA1)
27	PAD06	AN6 (RE1)	24	PAD02	AN2 (RA2)
26	PAD07	AN7 (RE2)	25	PAD03	AN3 (RA3)

JP13 – Port Header

#	HC12	PIC	#	HC12	PIC
50	+5V	+5V	1	PA7	RD7
49	Gnd	Gnd	2	PA6	RD6
48	PE7	NC	3	PA5	RD5
47	PK7	NC	4	PA4	RD4
46	PK5	NC	5	PA3	RD3
45	PK4	NC	6	PA2	RD2
44	PK3	NC	7	PA1	RD1
43	PK2	NC	8	PA0	RD0
42	PK1	NC	9	PB7	RC7
41	PK0	NC	10	PB6	RC6
40	PJ0	NC	11	PB5	RC5
39	PJ7	RC4	12	PB4	RC4
38	PJ6	RC3	13	PB3	RC3
37	PM7	NC	14	PB2	RC2
36	PM6	NC	15	PB1	RC1
35	PM5	NC	16	PB0	RC0
34	PM4	RE1	17	PE2	RE1
33	PM3	RE0	18	PE4	RE2
32	PM2	RE2	19	PE3	RE0
31	PM1	NC	20	PE1	RB0
30	PM0	NC	21	PJ1	NC
29	PAD14	NC	22	PAD10	AN0 (RA0)
28	PAD15	NC	23	PAD11	AN1 (RA1)
27	PAD16	NC	24	PAD12	AN2 (RA2)
26	PAD17	NC	25	PAD13	AN3 (RA3)

H1 &H2 – Micro-controller plug in location

- Plug micro-controller board in to these headers.
- Orientation of micro-controller boards is H1 to H1 and H2 to H2
- Reset switch on micro-controller board will be located at the back of the robot near H2

Rxa & RXB – RF. Comm. Header (Laipac Data Sheets)

#	*HC12*	*PIC*
1 – Gnd	Gnd	Gnd
2 – Digital Data Out	PS2	RC7
3 – Linear Out	NC	NC
4 - +5V	Controlled by PT3	Controlled by RB5
5 - +5V	Controlled by PT3	Controlled by RB5
6 - Gnd	Gnd	Gnd
7 – Gnd	Gnd	Gnd
8 - Antenna	NC	NC

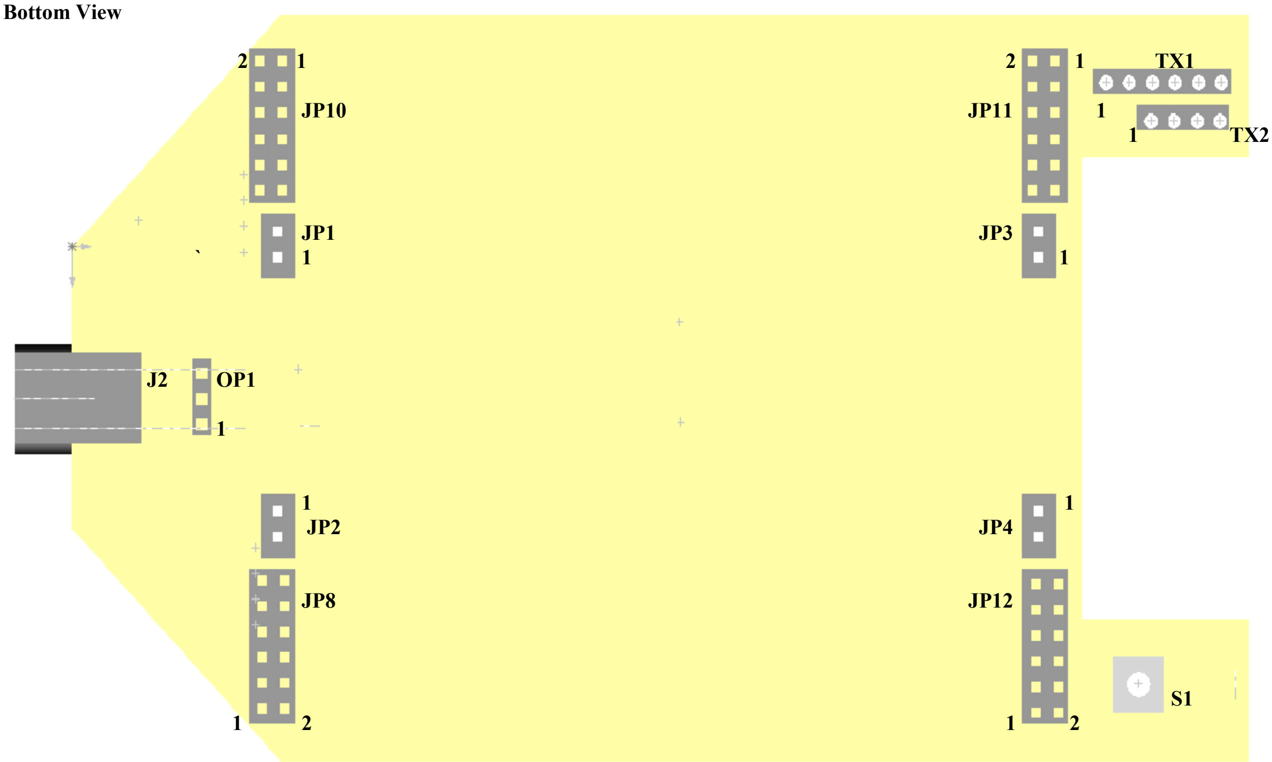
SV3- Motor Port (A3967 Stepper Motor Driver Data Sheet)

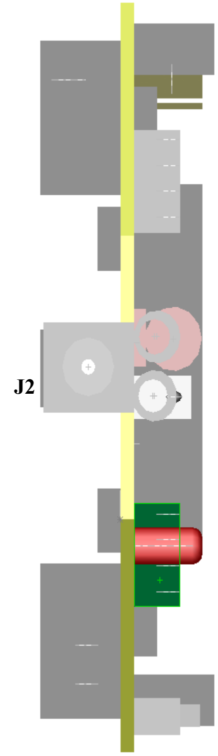
#	HC12	PIC	A3967 (pin – des)	#	HC12	PIC	A3967 (pin – des)
1	Gnd	Gnd		2	Gnd	Gnd	
3	Gnd	Gnd		4	Gnd	Gnd	
5	PP1 (AC coupled)	RC2 (AC coupled)	24-PFD	6	PT6	RC2	1-REF
7	PA6	RD6	3 -Sleep	8	PA7	RD7	22 - Reset
9	PT5	RB7	10-Step 2nd motor	10	PA5	RD5	11- Dir 2nd motor
11	PA2	RD2	12-MS1	12	PA3	RD3	13 – MS2
13	PT4	RB6	10 – Step 1st motor	14	PA1	RD1	11- Dir 1st motor
15	PAD11	NC		16	PAD10	AN2 (RA2)	
17	PAD15	NC		18	PAD12	NC	
19	+5V	+5V		20	+5V	+5V	
21	Vadj	Vadj		22	Vadj	Vadj	
23	+12V	+12 V		24	+12V	+12V	
25	Gnd	Gnd		26	Gnd	Gnd	

Sensors

#	*HC12*	*PIC*
1 – IR RX Mod (Data Sheet)	PS0 (Pulled high)	RC4 (Pulled high)
2 – Photo Resistor (Data Sheet)	PAD13	AN3 (RA3)
3 – IR Pin Diode (Data Sheet)	PAD03	AN3 (RA3)

Bottom View





Side View (from Front)

JP1, JP2, JP3, and JP4 – Battery Connectors

- 1 – Negative Terminal
- 2 – Positive Terminal
- Batteries are connected in series

JP10 – Sensor Header

#	HC12	PIC	#	HC12	PIC
1	PAD10	AN0 (RA0)	2	PAD11	AN1 (RA1)
3	PAD12	AN2 (RA2)	4	+5V	+5V
5	Gnd	Gnd	6	Gnd	Gnd
7	PT2	RB4	8	PB3	RC3
9	PB4	RC4	10	PB5	RC5
11	+14	+14V	12	+14V	+14V

JP8 – Sensor Header

#	HC12	PIC	#	HC12	PIC
1	PAD00	AN0 (RA0)	2	PAD01	AN1 (RA1)
3	PAD02	AN2 (RA2)	4	+5V	+5V
5	Gnd	Gnd	6	Gnd	Gnd
7	PT2	RB4	8	PH0	RB0
9	PH1	RB1	10	PH2	RB2
11	+14	+14V	12	+14V	+14V

JP11 – Sensor Header

#	HC12	PIC	#	HC12	PIC
1	PAD05	AN5 (RE0)	2	PAD06	AN6 (RE1)
3	Gnd	Gnd)	4	+5V	+5V
5	Gnd	Gnd	6	Gnd	Gnd
7	PT2	RB4	8	PP6	RA4
9	PP7	RA5	10	Gnd	Gnd
11	+14	+14V	12	+14V	+14V

JP12 – Sensor Header

#	HC12	PIC	#	HC12	PIC
1	PAD15	AN5 (RE0)	2	PAD16	AN6 (RE1)
3	Gnd	Gnd)	4	+5V	+5V
5	Gnd	Gnd	6	Gnd	Gnd
7	PT2	RB4	8	PP3	RA1
9	PP4	RA2	10	Gnd	Gnd
11	+14	+14V	12	+14V	+14V

***Tx1 – RF. Comm. Header** (Laipac Data Sheets)*

#	*HC12*	*PIC*
1	+5V	+5V
2	+5V	+5V
3	Gnd	Gnd
4	Gnd	Gnd
5	Antenna	Antenna
6 - Digital Data Input	PS3	RC6

***Tx2 – RF. Comm. Header** (Laipac Data Sheets)*

#	*HC12*	*PIC*
1	Gnd	Gnd
2 – Data In	PS3	RC6
3	+5V	+5V
4	Antenna	Antenna

***OP1 – IR Prox. Header** (Data Sheets)*

#	*HC12*	*PIC*
1 – Switched +5V	PT3	RB5
2	Analogue Gnd	Analogue Gnd
3 – prox out to 1.2k to PAD04 to 10k to gnd	PAD04	AN4 (RA5)

***S1 – Switch** (Pulled High through 10K)*

HC12	*PIC*
PS0	RC4

J2 – Charging Port

- 16V AC, 300mA
- Charging LED will light once Batteries reached full charge

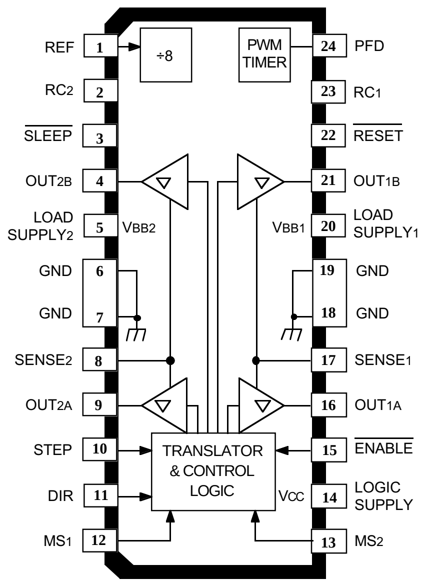
Power Sensing	*HC12*	*PIC*
Raw Charging Terminal	PE1	RB0
Logic Low on Full Charge	PE0	NC

3967

Data Sheet
26184.24

PRELIMINARY INFORMATION
(Subject to change without notice)
June 20, 2002

MICROSTEPPING DRIVER WITH TRANSLATOR



Dwg. PP-075-2

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

Load Supply Voltage, V_{BB} .... **30 V**
Output Current, I_{OUT}
  Continuous .... **±750 mA***
  Peak .... **±850 mA**
Logic Supply Voltage, V_{CC} .... **7.0 V**
Logic Input Voltage Range, V_{IN}
  (t_w >30 ns) .... **-0.3 V to V_{CC} + 0.3 V**
  (t_w <30 ns) .... **-1 V to V_{CC} + 1 V**
Sense Voltage, V_{SENSE} .... **0.68 V**
Reference Voltage, V_{REF} .... **V_{CC}**
Package Power Dissipation,
  P_D .... **2.2 W**
Operating Temperature Range,
  T_A .... **-20°C to +85°C**
Junction Temperature, T_J .... **+150°C**
Storage Temperature Range,
  T_S .... **-55°C to +150°C**

* Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

The A3967SLB is a complete microstepping motor driver with built-in translator. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and eighth-step modes, with output drive capability of 30 V and ±750 mA. The A3967SLB includes a fixed off-time current regulator that has the ability to operate in slow, fast, or mixed current-decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

The translator is the key to the easy implementation of the A3967SLB. By simply inputting one pulse on the STEP input the motor will take one step (full, half, quarter, or eighth depending on two logic inputs). There are no phase-sequence tables, high-frequency control lines, or complex interfaces to program. The A3967SLB interface is an ideal fit for applications where a complex µP is unavailable or over-burdened.

Internal circuit protection includes thermal shutdown with hysteresis, under-voltage lockout (UVLO) and crossover-current protection. Special power-up sequencing is not required.

The A3967SLB is supplied in a 24-lead SOIC with copper batwing tabs. The tabs are at ground potential and need no insulation.

FEATURES

- ±750 mA, 30 V Output Rating
- Satlington™ Sink Drivers
- Automatic Current-Decay Mode Detection/Selection
- 3.0 V to 5.5 V Logic Supply Voltage Range
- Mixed, Fast, and Slow Current-Decay Modes
- Internal UVLO and Thermal Shutdown Circuitry
- Crossover-Current Protection

Always order by complete part number, e.g., **A3967SLB** .

FUNCTIONAL BLOCK DIAGRAM

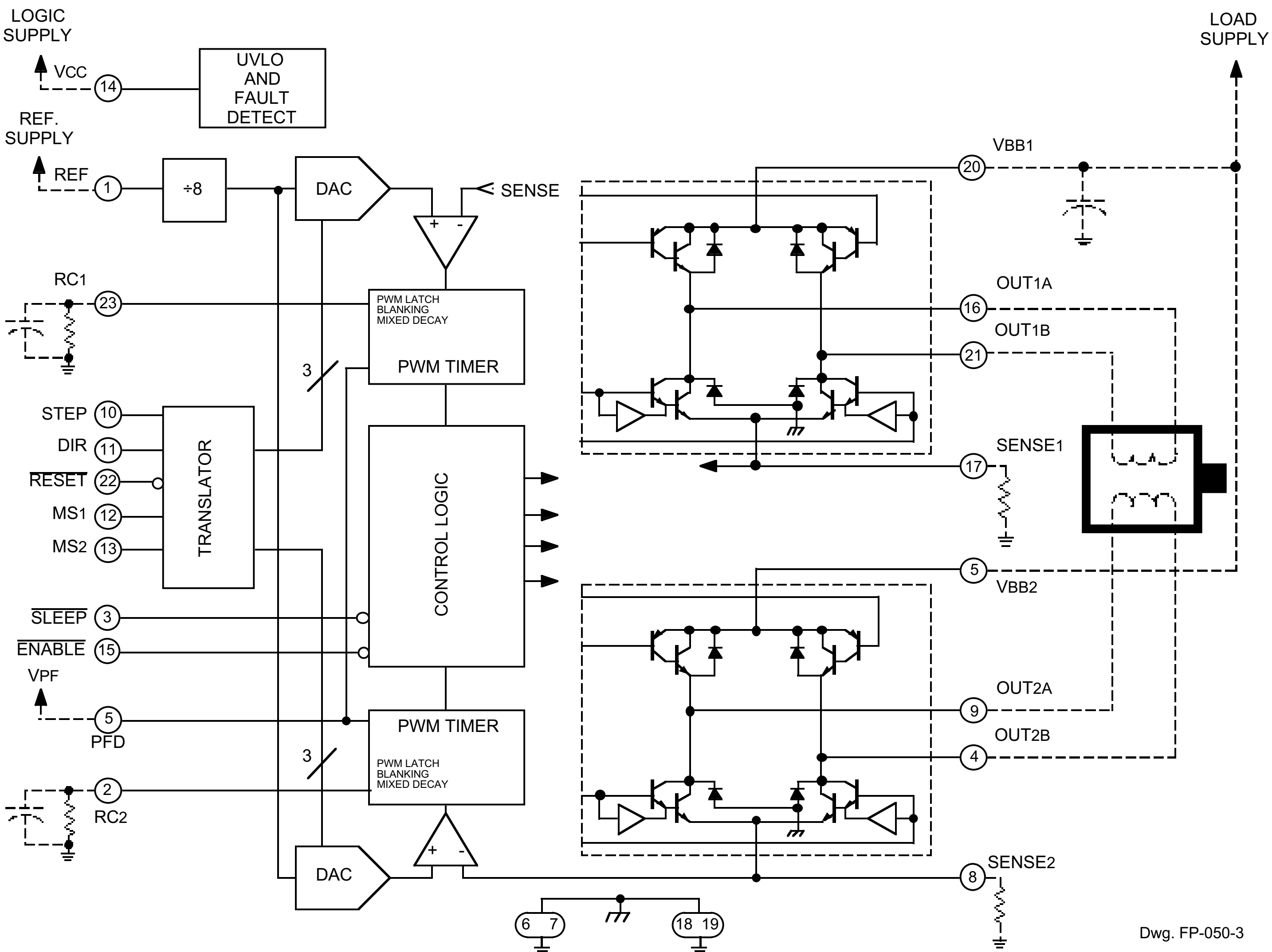


Table 1. Microstep Resolution Truth Table

MS_1	MS_2	Resolution
L	L	Full step (2 phase)
H	L	Half step
L	H	Quarter step
H	H	Eighth step

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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 30 V, V_{CC} = 3.0 V to 5.5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	4.75	–	30	V
		During sleep mode	0	–	30	V
Output Leakage Current	I_{CEX}	$V_{OUT} = V_{BB}$	–	<1.0	20	µA
		V_{OUT} = 0 V	–	<-1.0	-20	µA
Output Saturation Voltage	$V_{CE(sat)}$	Source driver, I_{OUT} = -750 mA	–	–	2.1	V
		Source driver, I_{OUT} = -400 mA	–	–	2.0	V
		Sink driver, I_{OUT} = 750 mA	–	–	1.3	V
		Sink driver, I_{OUT} = 400 mA	–	–	0.5	V
Clamp Diode Forward Voltage	V_F	I_F = 750 mA	–	1.4	1.6	V
		I_F = 400 mA	–	1.1	1.4	V
Motor Supply Current	I_{BB}	Outputs enabled	–	–	5.0	mA
		RESET high	–	–	200	µA
		Sleep mode	–	–	20	µA
Control Logic						
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
Logic Input Voltage	$V_{IN(1)}$		$0.7V_{DD}$	–	–	V
	$V_{IN(0)}$		–	–	$0.3V_{DD}$	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = 0.7V_{DD}$	-20	<1.0	20	µA
	$I_{IN(0)}$	$V_{IN} = 0.3V_{DD}$	-20	<1.0	20	µA
Maximum STEP Frequency	f_{STEP}		500*	–	–	kHz
Blank Time	t_{BLANK}	R_t = 56 kΩ, C_t = 680 pF	700	950	1200	ns
Fixed Off Time	t_{off}	R_t = 56 kΩ, C_t = 680 pF	30	38	46	µs

continued next page …

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 30 V, V_{DD} = 3.0 V to 5.5V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Control Logic (cont'd)						
Mixed Decay Trip Point	PFDH		–	$0.6V_{CC}$	–	V
	PFDL		–	$0.21V_{CC}$	–	V
Ref. Input Voltage Range	V_{REF}	Operating	1.0	–	V_{CC}	V
Reference Input Impedance	Z_{REF}		120	160	200	kΩ
Gain (G_m) Error (note 3)	E_G	V_{REF} = 2 V, Step = 3†	–	–	±10	%
		V_{REF} = 2 V, Step = 5†	–	–	±5.0	%
		V_{REF} = 2 V, Step = 9†	–	–	±5.0	%
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	15	–	°C
UVLO Enable Threshold	V_{UVLO}	Increasing V_{DD}	2.45	2.7	2.95	V
UVLO Hysteresis	ΔV_{UVLO}		0.05	0.10	–	V
Logic Supply Current	I_{DD}	Outputs enabled	–	65	85	mA
		Outputs off	–	–	9.0	mA
		Sleep mode	–	–	100	µA

* Operation at a step frequency greater than the specified minimum value is possible but not warranteed.
† 8 microstep/step operation.

NOTES:
1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.
3. $E_G = ([V_{REF}/8] - V_{SENSE})/(V_{REF}/8)$

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Functional Description

Device Operation. The A3967 is a complete microstepping motor driver with built in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter- and eighth-step modes. The current in each of the two output H-bridges is regulated with fixed off time pulse-width modulated (PWM) control circuitry. The H-bridge current at each step is set by the value of an external current sense resistor (R_S), a reference voltage (V_{REF}), and the DAC's output voltage controlled by the output of the translator.

At power up, or reset, the translator sets the DACs and phase current polarity to initial home state (see figures for home-state conditions), and sets the current regulator for both phases to mixed-decay mode. When a step command signal occurs on the STEP input the translator automatically sequences the DACs to the next level (see table 2 for the current level sequence and current polarity). The microstep resolution is set by inputs MS_1 and MS_2 as shown in table 1. If the new DAC output level is lower than the previous level the decay mode for that H-bridge will be set by the PFD input (fast, slow or mixed decay). If the new DAC level is higher or equal to the previous level then the decay mode for that H-bridge will be slow decay. This automatic current-decay selection will improve microstepping performance by reducing the distortion of the current waveform due to the motor BEMF.

Reset Input ($\overline{\text{RESET}}$). The RESET input (active low) sets the translator to a predefined home state (see figures for home state conditions) and turns off all of the outputs. STEP inputs are ignored until the RESET input goes high.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the state of inputs MS_1 and MS_2 (see table 1).

Microstep Select (MS_1 and MS_2). Input terminals MS1 and MS_2 select the microstepping format per table 1. Changes to these inputs do not take effect until the STEP command (see figure).

Direction Input (DIR). The state of the DIRECTION input will determine the direction of rotation of the motor.

Internal PWM Current Control. Each H-bridge is controlled by a fixed off time PWM current-control circuit that limits the load current to a desired value (I_{TRIP}). Initially, a diagonal pair of source and sink outputs are enabled and current flows through the motor winding and R_S. When the voltage across the current-sense resistor equals the DAC output voltage, the current-sense comparator resets the PWM latch, which turns off the source driver (slow-decay mode) or the sink and source drivers (fast- or mixed-decay modes).

The maximum value of current limiting is set by the selection of R_S and the voltage at the V_{REF} input with a transconductance function approximated by:

$$I_{TRIP}\text{max} = V_{REF}/8R_S$$

The DAC output reduces the V_{REF} output to the current-sense comparator in precise steps (see table 2 for % I_{TRIP}max at each step).

$$I_{TRIP} = (\%\ I_{TRIP}\text{max}/100) \times I_{TRIP}\text{max}$$

Fixed Off-Time. The internal PWM current-control circuitry uses a one shot to control the time the driver(s) remain(s) off. The one shot off-time, t_{off}, is determined by the selection of an external resistor (R_T) and capacitor (C_T) connected from the RC timing terminal to ground. The off time, over a range of values of C_T = 470 pF to 1500 pF and R_T = 12 kΩ to 100 kΩ is approximated by:

$$t_{off} = R_T C_T$$

Functional Description (cont'd)

RC Blanking. In addition to the fixed off time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry. The comparator output is blanked to prevent false over-current detection due to reverse recovery currents of the clamp diodes, and/or switching transients related to the capacitance of the load. The blank time t_{BLANK} can be approximated by:

$$t_{BLANK} = 1400C_T$$

Enable Input ($\overline{\text{ENABLE}}$). This active-low input enables all of the outputs. When logic high the outputs are disabled. Inputs to the translator (STEP, DIRECTION, MS_1, MS_2) are all active independent of the ENABLE input state.

Shutdown. In the event of a fault (excessive junction temperature) the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{CC}, the under-voltage lockout (UVLO) circuit disables the drivers and resets the translator to the home state.

Sleep Mode ($\overline{\text{SLEEP}}$). An active-low control input used to minimize power consumption when not in use. This disables much of the internal circuitry including the outputs. A logic high allows normal operation and startup of the device in the home position.

Percent Fast Decay Input (PFD). When a STEP input signal commands a lower output current from the previous step, it switches the output current decay to either slow-, fast-, or mixed-decay depending on the voltage level at the PFD input. If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

Mixed Decay Operation. If the voltage on the PFD input is between $0.6V_{DD}$ and $0.21V_{DD}$, the bridge will operate in mixed-decay mode depending on the step sequence (see figures). As the trip point is reached, the device will go into fast-decay mode until the voltage on the RC terminal decays to the voltage applied to the PFD terminal. The time that the device operates in fast decay is approximated by:

$$t_{FD} = R_TC_T\ln (0.6V_{DD}/V_{PFD})$$

After this fast decay portion, t_{FD}, the device will switch to slow-decay mode for the remainder of the fixed off-time period.

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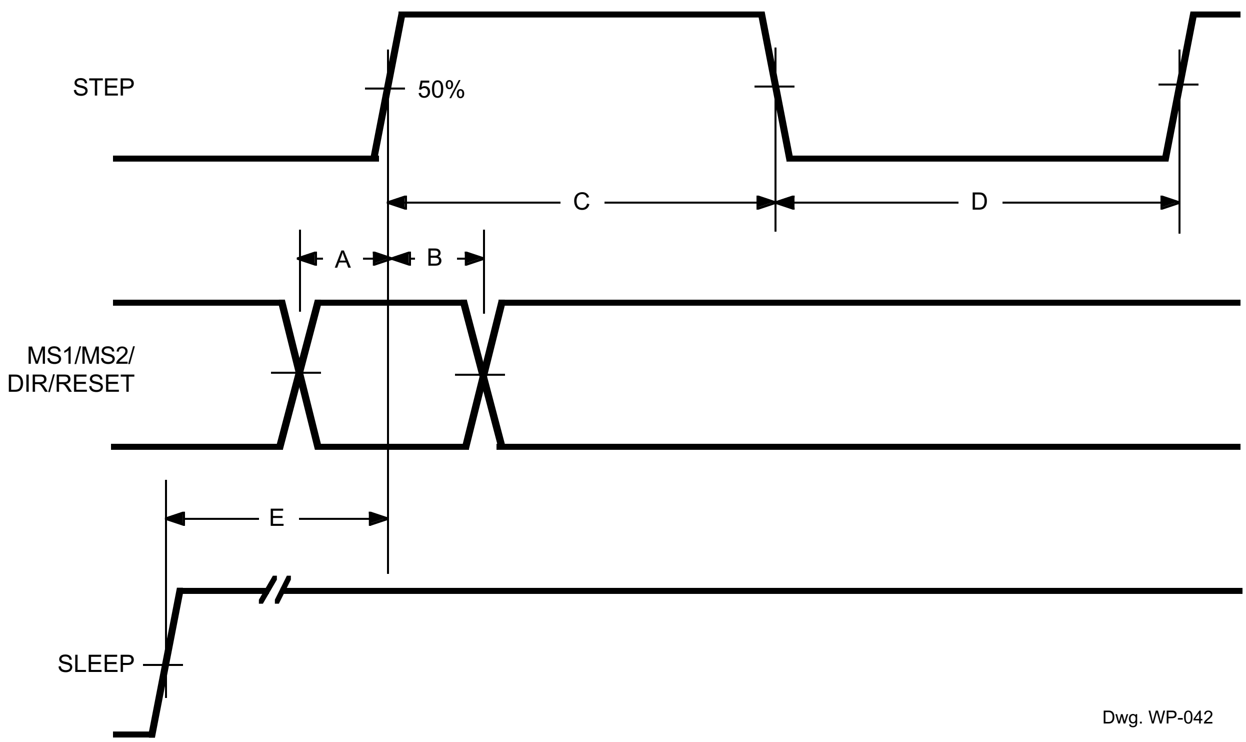
Timing Requirements

(T_A = +25°C, V_{CC} = 5 V, Logic Levels are V_{CC} and Ground)



A. Minimum Command Active Time
Before Step Pulse (Data Set-Up Time) ..... 200 ns

B. Minimum Command Active Time
After Step Pulse (Data Hold Time) .... 200 ns

C. Minimum STEP Pulse Width .... 1.0 µs

D. Minimum STEP Low Time .... 1.0 µs

E. Maximum Wake-Up Time .... 1.0 ms

Applications Information

Layout. The printed wiring board should use a heavy ground plane.

For optimum electrical and thermal performance, the driver should be soldered directly onto the board.

The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (>47 µF is recommended) placed as close to the device as possible.

To avoid problems due to capacitive coupling of the high dv/dt switching transients, route the bridge-output traces away from the sensitive logic-input traces. Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. A star ground system located close to the driver is recommended.

The 24-lead SOIC has the analog ground and the power ground internally bonded to the power tabs of the package (leads 6, 7, 18, and 19).

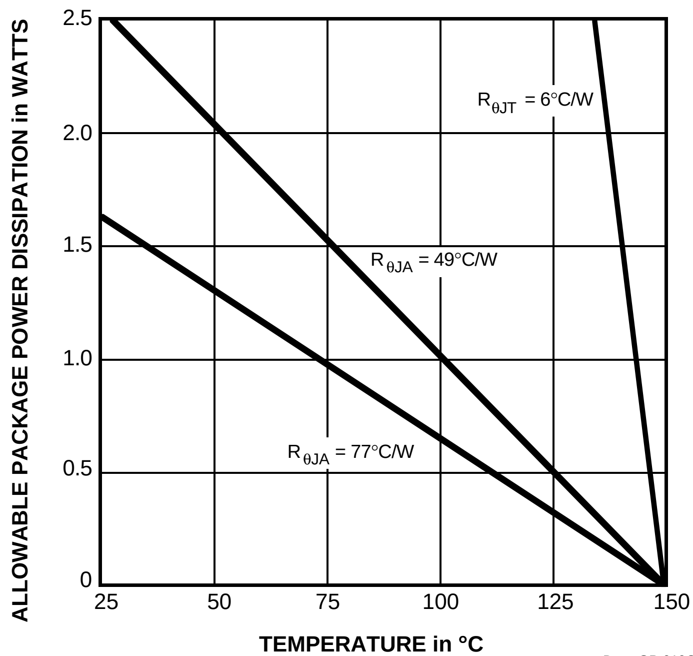
Current Sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistor (R_S) should have an independent ground return to the star ground of the device. This path should be as short as possible. For low-value sense resistors the IR drops in the printed wiring board sense resistor's traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

Allegro MicroSystems recommends a value of R_S given by

$$R_S = 0.5/I_{TRIP}max$$

Thermal protection. Circuitry turns off all drivers when the junction temperature reaches 165°C, typically. It is intended only to protect the device from failures due to excessive junction temperatures and should not imply that output short circuits are permitted. Thermal shut-down has a hysteresis of approximately 15°C.

$R_{\theta JA}$ is measured on typical two-sided PCB with minimal copper ground area (77°C/W) or with 3.57 in^2 copper ground area (49°C/W). See also, Application Note 29501.5, *Improving Batwing Power Dissipation*.



Dwg. GP-019C

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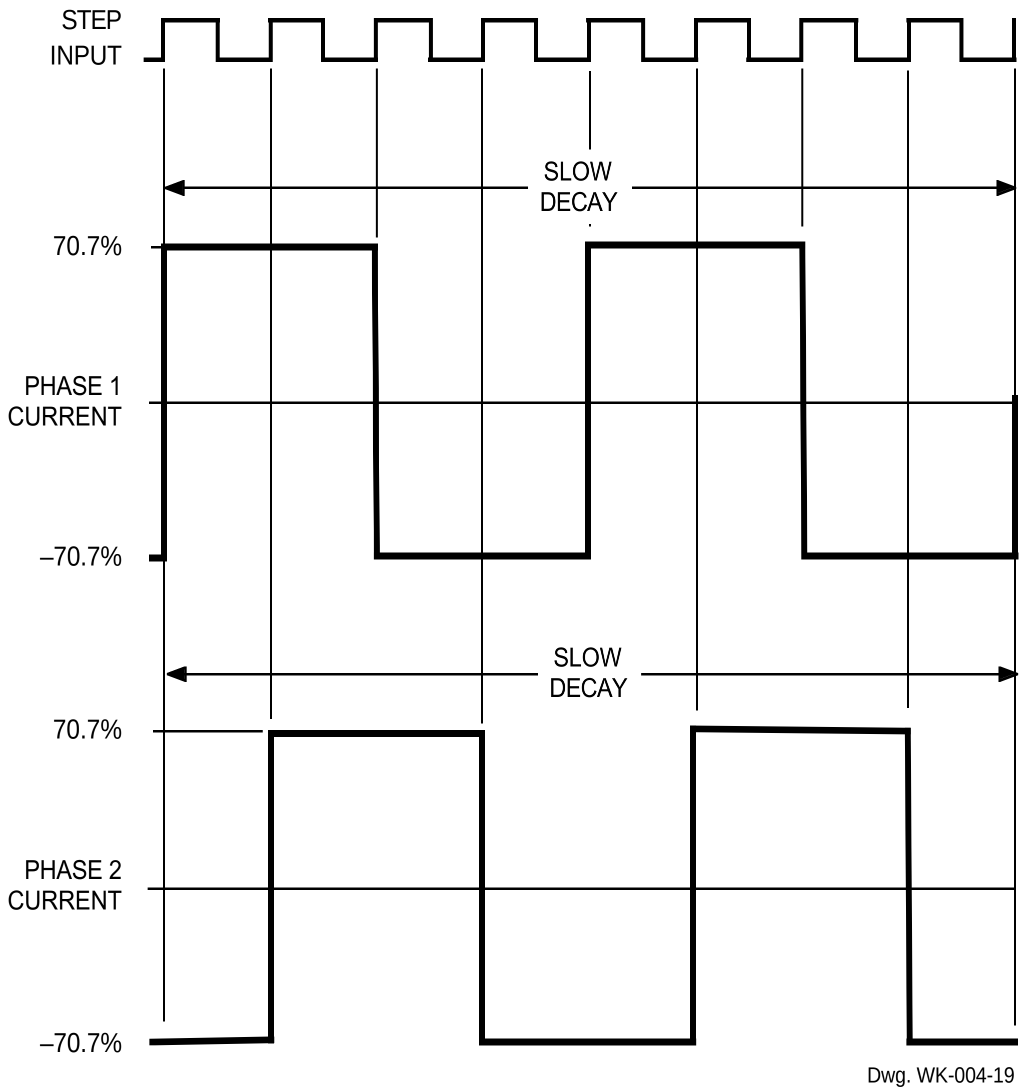
Table 2. Step Sequencing
(DIR = L)

Full Step #	Half Step #	Quarter Step #	Eighth Step #	Phase 2 Current [%I_{trip}max]	Phase 1 Current [%I_{trip}max]	Step Angle
	1	1	1	0.00	100.00	0
			2	19.51	98.08	11.25
		2	3	38.27	92.39	22.50
			4	55.56	83.15	33.75
1	2	3	5	70.71	70.71	45*
			6	83.15	55.56	56.25
		4	7	92.39	38.27	67.50
			8	98.08	19.51	78.75
	3	5	9	100.00	0.00	90
			10	98.08	-19.51	101.25
		6	11	92.39	-38.27	112.50
			12	83.15	-55.56	123.75
2	4	7	13	70.71	-70.71	135
			14	55.56	-83.15	146.25
		8	15	38.27	-92.39	157.50
			16	19.51	-98.08	168.75
	5	9	17	0.00	-100.00	180
			18	-19.51	-98.08	191.25
		10	19	-38.27	-92.39	202.50
			20	-55.56	-83.15	213.75
3	6	11	21	-70.71	-70.71	225
			22	-83.15	-55.56	236.25
		12	23	-92.39	-38.27	247.50
			24	-98.08	-19.51	258.75
	7	13	25	-100.00	0.00	270
			26	-98.08	19.51	281.25
		14	27	-92.39	38.27	292.50
			28	-83.15	55.56	303.75
4	8	15	29	-70.71	70.71	315
			30	-55.56	83.15	326.25
		16	31	-38.27	92.39	337.50
			32	-19.51	98.08	348.75
	9	17	33	0.00	100.00	360

* Home state.

Full Step Operation
$MS_1 = MS_2 = L$, DIR = H



The vector addition of the output currents at any step is 100%.

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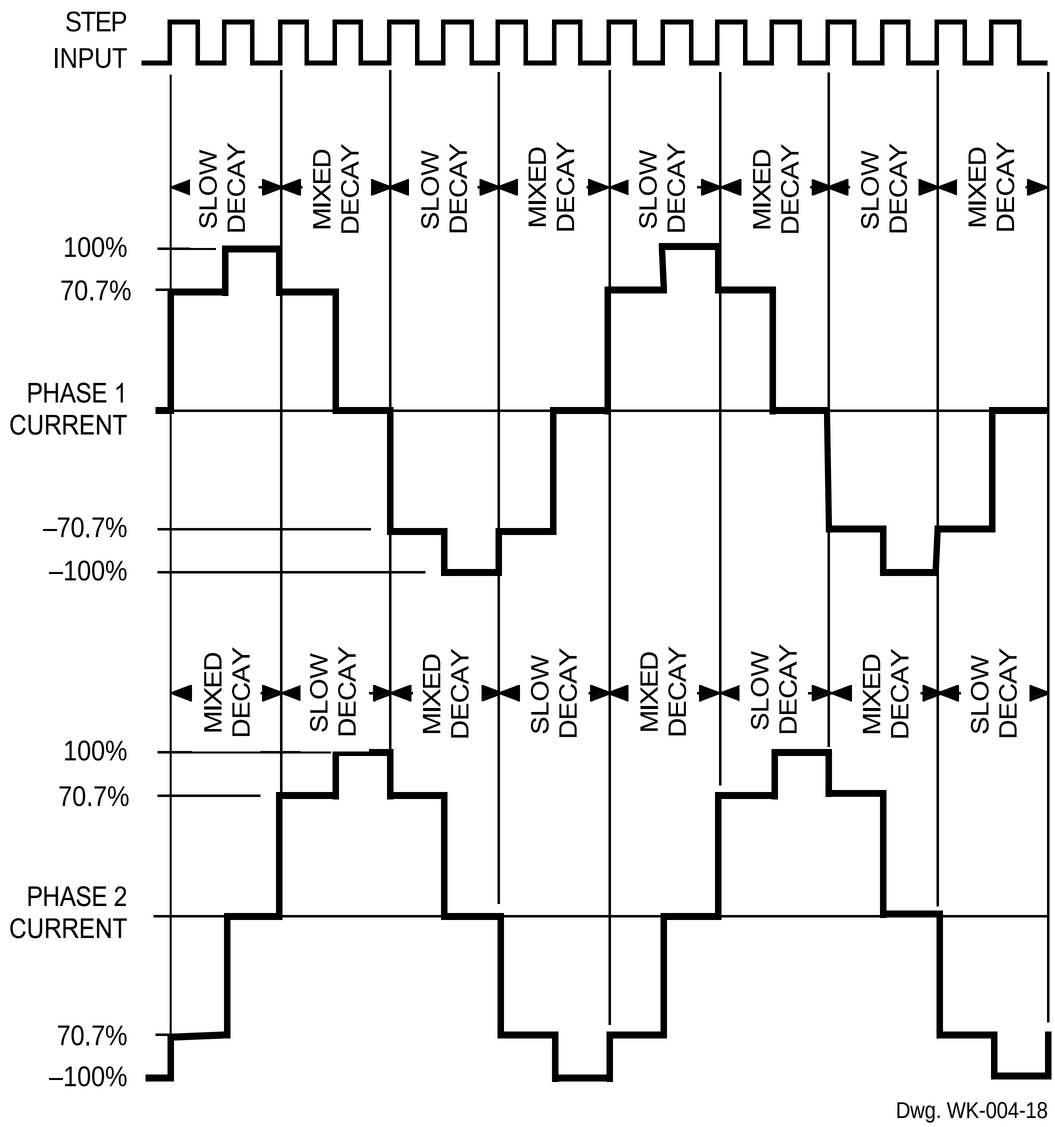
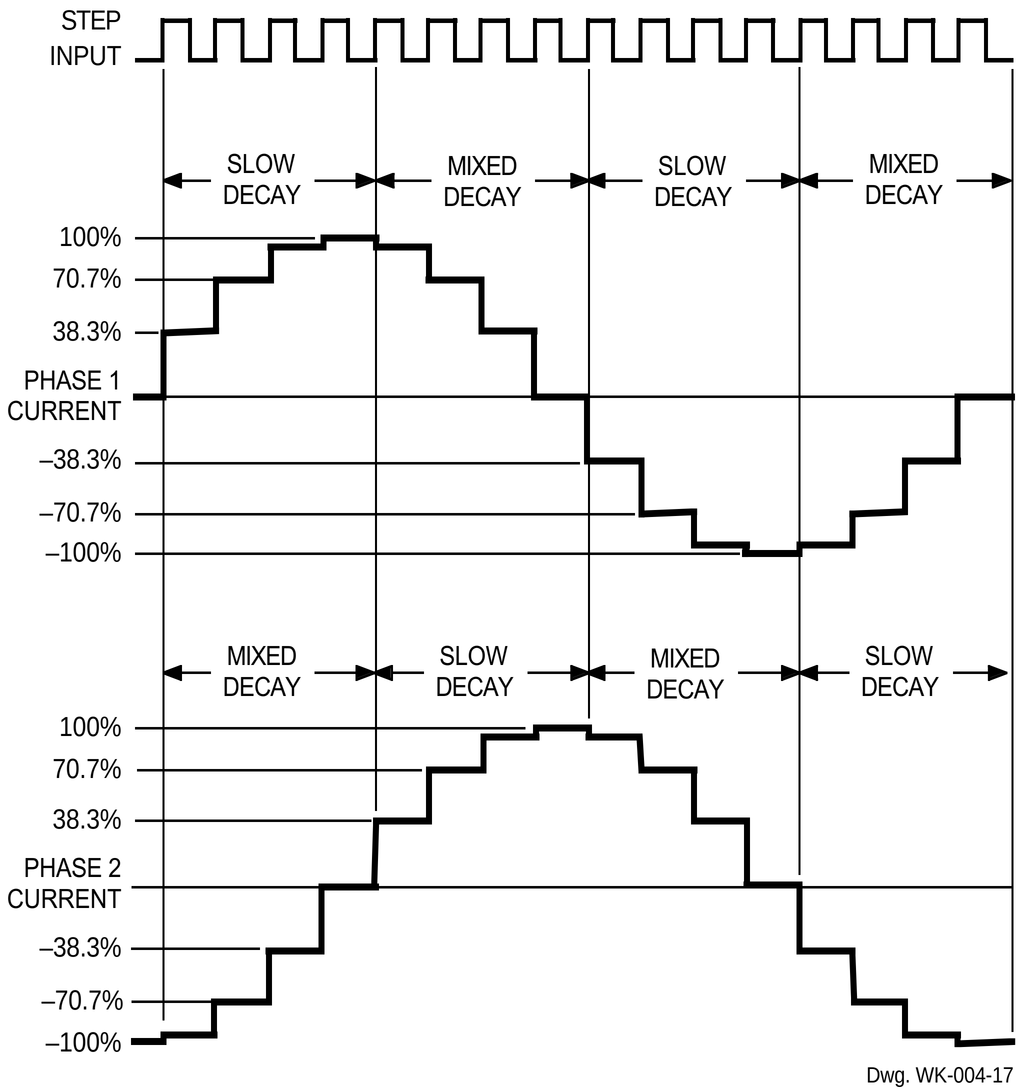
Half Step Operation

MS_1 = H, MS_2 = L, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

Quarter Step Operation
MS_1 = L, MS_2 = H, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

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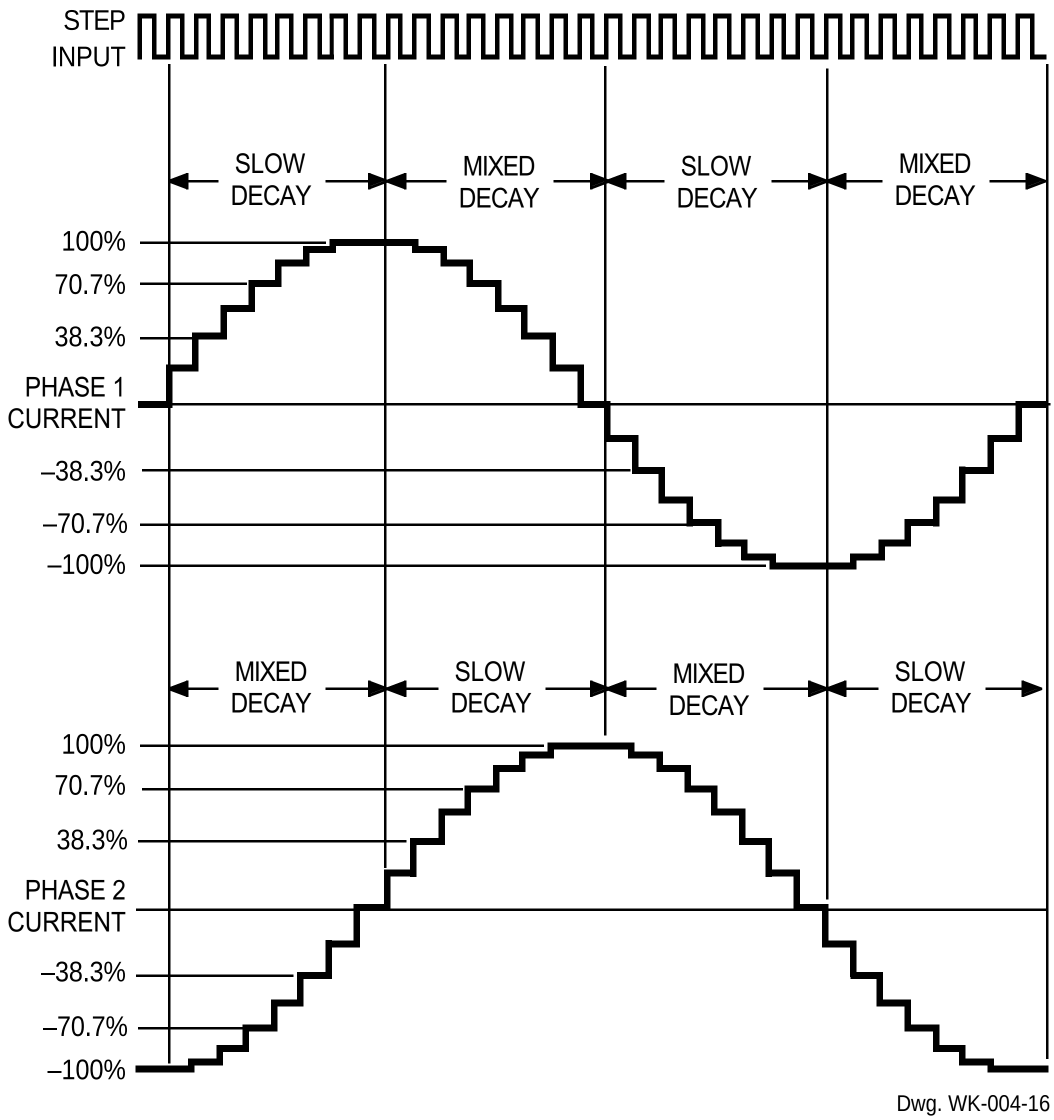
8 Microstep/Step Operation
$MS_1 = MS_2 = H$, DIR = H



The mixed-decay mode is controlled by the percent fast decay voltage (V_{PFD}). If the voltage at the PFD input is greater than $0.6V_{DD}$ then slow-decay mode is selected. If the voltage on the PFD input is less than $0.21V_{DD}$ then fast-decay mode is selected. Mixed decay is between these two levels.

Terminal List

Terminal Name	Terminal Description	Terminal Number
REF	Gm reference input	1
RC2	Analog input for fixed offtime – bridge 2	2
SLEEP	Logic input	3
OUT2B	H bridge 2 output B	4
LOAD SUPPLY2	VBB2, the load supply for bridge 2	5
GND	Analog and power ground	6, 7
SENSE2	Sense resistor for bridge 2	8
OUT2A	H bridge 2 output A	9
STEP	Logic input	10
DIR	Logic Input	11
MS1	Logic input	12
MS2	Logic input	13
LOGIC SUPPLY	VCC, the logic supply voltage	14
ENABLE	Logic input	15
OUT1A	H bridge 1 output A	16
SENSE1	Sense resistor for bridge 1	17
GND	Analog and power ground	18, 19
LOAD SUPPLY1	VBB1, the load supply for bridge 1	20
OUT1B	H bridge 1 output B	21
RESET	Logic input	22
RC1	Analog Input for fixed offtime – bridge 1	23
PFD	Mixed decay setting	5

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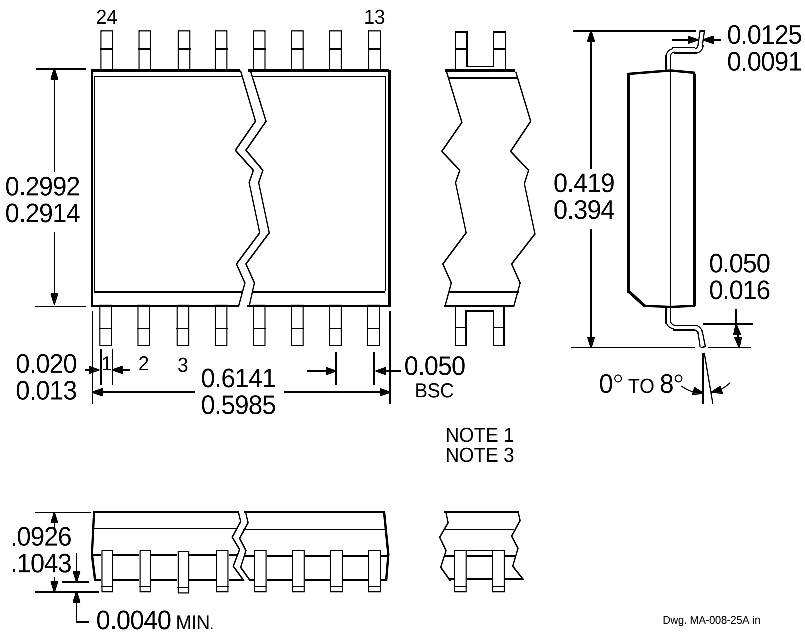
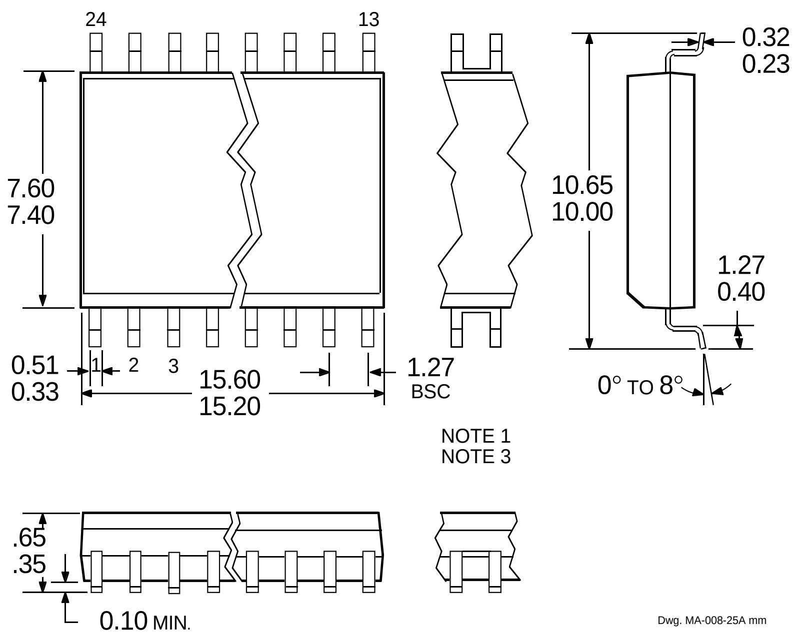


Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.
4. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

MOTOR DRIVERS

Function	Output Ratings*		Part Number†
INTEGRATED CIRCUITS FOR BRUSHLESS DC MOTORS			
3-Phase Power MOSFET Controller	—	28 V	3933
3-Phase Power MOSFET Controller	—	50 V	3932
3-Phase Back-EMF Controller/Driver	±900 mA	14 V	8902–A
INTEGRATED BRIDGE DRIVERS FOR DC AND BIPOLAR STEPPER MOTORS			
Dual Full Bridge with Protection & Diagnostics	±500 mA	30 V	3976
PWM Current-Controlled Dual Full Bridge	±650 mA	30 V	3966
PWM Current-Controlled Dual Full Bridge	±650 mA	30 V	3968
Microstepping Translator/Dual Full Bridge	±750 mA	30 V	3967
PWM Current-Controlled Dual Full Bridge	±750 mA	45 V	2916
PWM Current-Controlled Dual Full Bridge	±750 mA	45 V	2919
PWM Current-Controlled Dual Full Bridge	±750 mA	45 V	6219
PWM Current-Controlled Dual Full Bridge	±800 mA	33 V	3964
PWM Current-Controlled Dual DMOS Full Bridge	±1.0 A	35 V	3973
PWM Current-Controlled Full Bridge	±1.3 A	50 V	3953
PWM Current-Controlled Dual Full Bridge	±1.5 A	45 V	2917
PWM Current-Controlled DMOS Full Bridge	±1.5 A	50 V	3948
PWM Current-Controlled Microstepping Full Bridge	±1.5 A	50 V	3955
PWM Current-Controlled Microstepping Full Bridge	±1.5 A	50 V	3957
PWM Current-Controlled Dual DMOS Full Bridge	±1.5 A	50 V	3972
PWM Current-Controlled Dual DMOS Full Bridge	±1.5 A	50 V	3974
PWM Current-Controlled Full Bridge	±2.0 A	50 V	3952
PWM Current-Controlled DMOS Full Bridge	±2.0 A	50 V	3958
Microstepping Translator/Dual DMOS Full Bridge	±2.5 A	35 V	3977
Dual DMOS Full Bridge	±2.5 A	50 V	3971
PWM Current-Controlled DMOS Full Bridge	±3.0 A	50 V	3959
UNIPOLAR STEPPER MOTOR & OTHER DRIVERS			
Unipolar Stepper-Motor Quad Drivers	1.0 A	46 V	7024 & 7029
Unipolar Microstepper-Motor Quad Driver	1.2 A	46 V	7042
Unipolar Stepper-Motor Translator/Driver	1.25 A	50 V	5804
Unipolar Stepper-Motor Quad Driver	1.8 A	50 V	2540
Unipolar Stepper-Motor Quad Driver	3.0 A	46 V	7026
Unipolar Microstepper-Motor Quad Driver	3.0 A	46 V	7044

* Current is maximum specified test condition, voltage is maximum rating. See specification for sustaining voltage limits or over-current protection voltage limits. Negative current is defined as coming out of (sourcing) the output.

† Complete part number includes additional characters to indicate operating temperature range and package style.

Also, see 3175, 3177, 3235, and 3275 Hall-effect sensors for use with brushless dc motors.

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Representative photograph, actual product appearance may vary.

Dimensions

Schematic

Performance Charts

Specifications

Click here for a print friendly version of this datasheet.

SDP8436-003

SDP Series Silicon PhotoTransistor, Side-looking Plastic Package

Features

- Side-looking plastic package
- 18 ° (nominal) acceptance angle
- Enhanced coupling distance
- Internal visible light rejection filter
- Low profile for design flexibility
- Wide sensitivity ranges
- Mechanically matched to SEP8736 infrared emitting diodes

Description

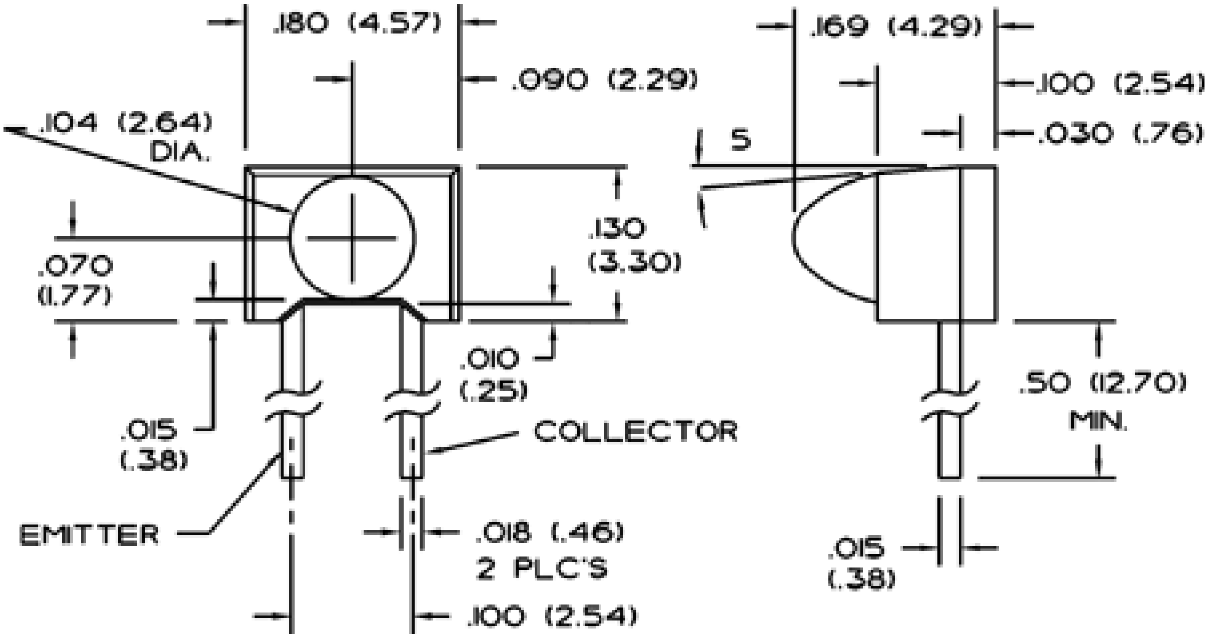
The SDP8436 is an NPN silicon phototransistor molded in a black plastic package which combines the mounting advantages of a side-looking package with the narrow acceptance angle and high optical gain of a T-1 package. The SDP8436 is designed for those applications which require longer coupling distances than standard side-looking devices can provide, such as touch screens. The device is also well suited to applications in which adjacent channel crosstalk could be a problem. The package is highly transmissive to the IR source energy while it provides effective shielding against visible ambient light.

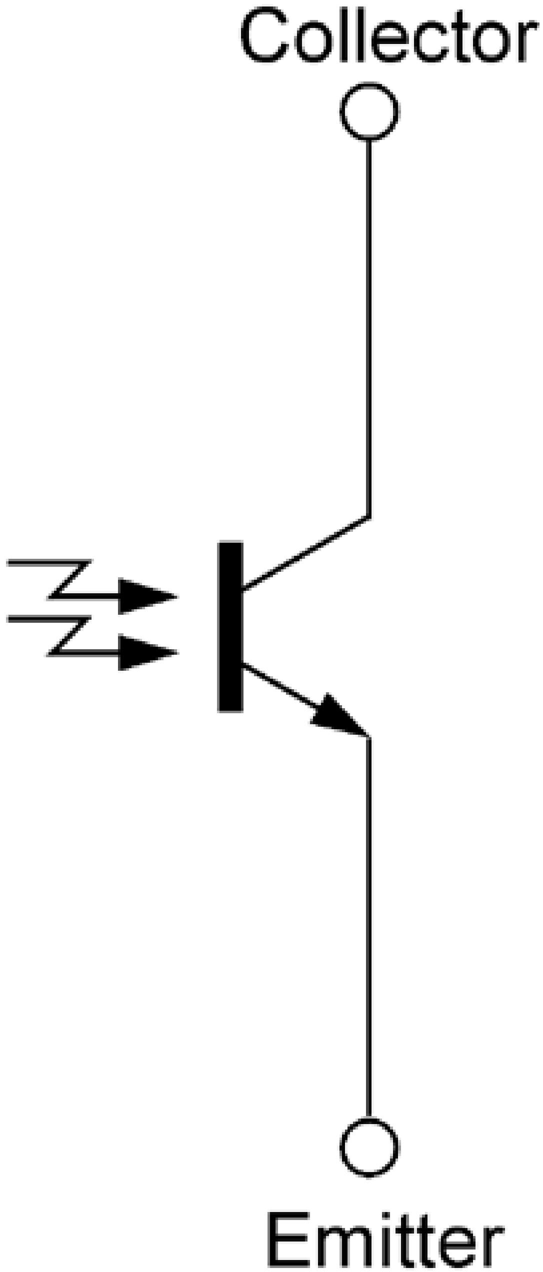
Product Specifications	
Product Type	IR Component
Angular Response (Degree)	18
Light Current Minimum	7.0 mA
Light Current Maximum	17.5 mA
Package Style	Side-Looking
Package Components	Plastic
Package Color	Black
Rise and Fall Time	15 µs
Power Dissipation	100 mW
Operating Temperature Range	-40 °C to 85 °C [-40 °F to 185 °F]
Dark Current	100 nA
Collector-Emitter Breakdown Voltage	30 V
Emitter-Collector Breakdown Voltage	5 V
Collector-Emitter Saturation Voltage	0.4 V
Comment	The radiation source is a tungsten lamp operating at a color temperature of 2870°K.
Availability	Global
Product Name	Phototransistor

Due to regional agency approval requirements, some products may not be available in your area.
Please contact your regional Honeywell office regarding your product of choice.

Top of Page

Please send comments to webmaster.sc@honeywell.com

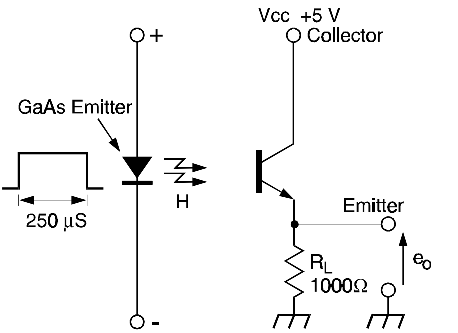

.180 (4.57)
.090 (2.29)
.104 (2.64) DIA.
.070 (1.77)
.130 (3.30)
.010 (.25)
.015 (.38)
COLLECTOR
EMITTER
.018 (.46) 2 PLC'S
.100 (2.54)
.169 (4.29)
.100 (2.54)
.030 (.76)
5
.50 (12.70) MIN.
.015 (.38)


Collector
Emitter

SDP8436
Silicon Phototransistor

SWITCHING TIME TEST CIRCUIT

cir_015.cdr



SWITCHING WAVEFORM

cir_004.cdr

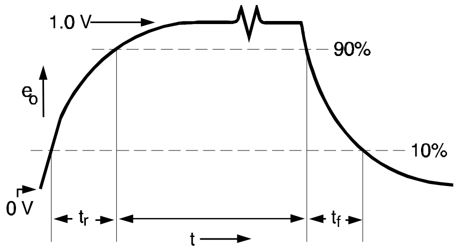


Fig. 1 Responsivity vs Angular Displacement

gra_013.ds4

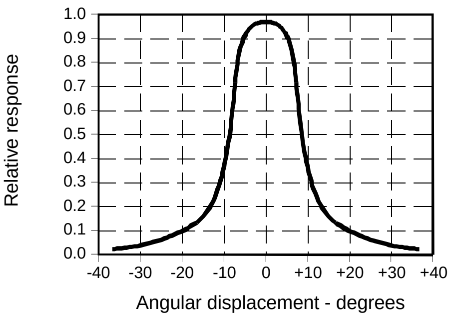


Fig. 2 Collector Current vs Ambient Temperature

gra_039.ds4

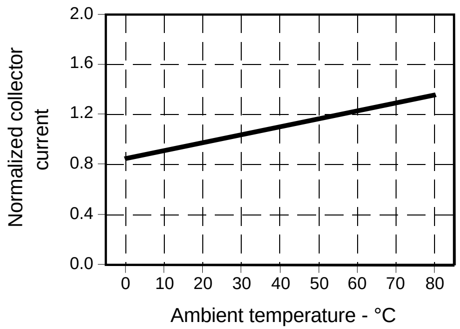


Fig. 3 Dark Current vs Temperature

gra_301.cdr

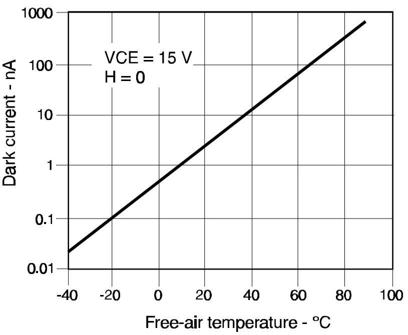
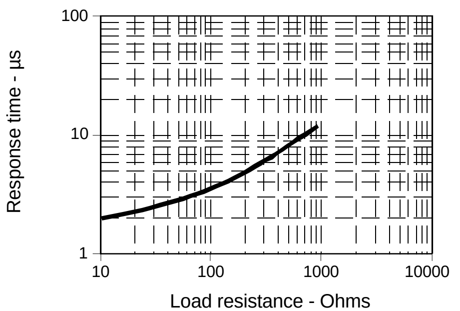


Fig. 4 Non-Saturated Switching Time vs Load Resistance

gra_041.ds4



SDP8436

Silicon Phototransistor

Fig. 5 Spectral Responsivity

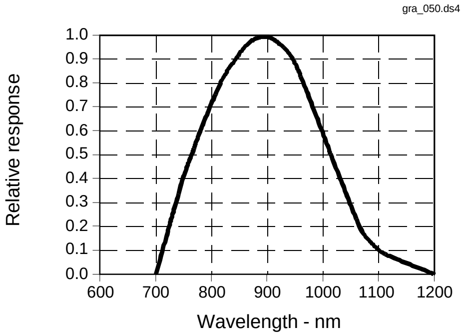
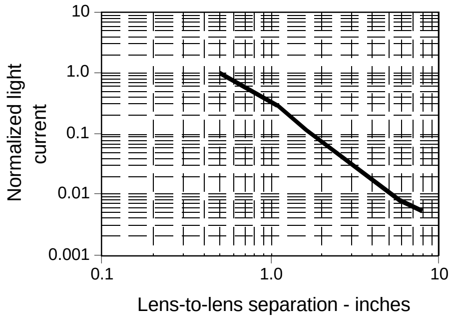


Fig. 6 Coupling Characteristics with SEP8736

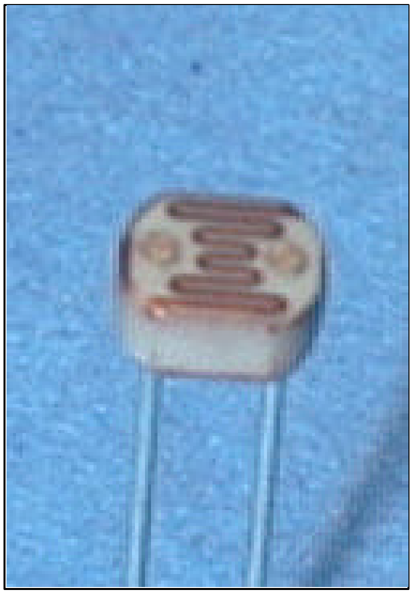


All Performance Curves Show Typical Values

PHOTONIC DETECTORS INC.

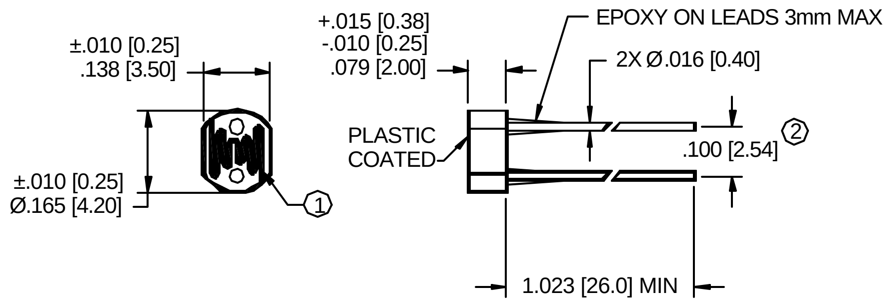
Cadmium Sulfoselenide (CdS) Photoconductive Photocells

Type PDV-P9XXX-X



PACKAGE DIMENSIONS INCH [mm]

INDUSTRY EQUIVALENTS: VT900 & NSL5152



PLASTIC COATED CERAMIC PACKAGE

1. PHOTOCELL "GRID" PATTERN CAN VARY, PDI RESERVES THE RIGHT TO CHANGE AND MIX GRID PATTERNS.
2. DIMENSION CONTROLLED AT BASE OF CERAMIC HEADER PACKAGE.

FEATURES

- Visible light response
- Sintered construction
- Low cost
- High Reliability

DESCRIPTION

PDV-P9XXX-X are (CdS) photoconductive photocells designed to sense light from 400 nm to 700 nm. As light dependent resistors, they are available in a wide range of resistance values. They are packaged in a two leaded plastic-coated ceramic header.

APPLICATIONS

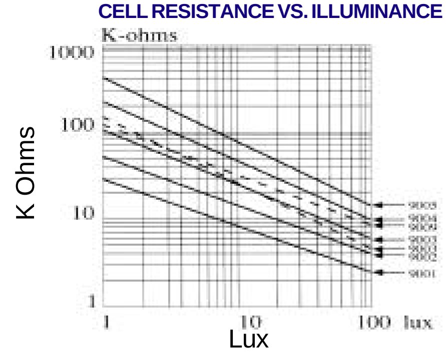
- Camera exposure
- Low light level
- Shutter controls
- Night light controls

ABSOLUTE MAXIMUM RATING (TA=25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{PK}	Applied Voltage		150	V dc
$P_{d\Delta\ po\Delta t}$	Continuous Power Dissipation		90	mW/°C
T_{stg} & T_o	Operating Temperature Range & Storage	-30	+75	°C
T_S	Soldering Temperature*		+260	°C

*.200 inch (5 mm) from bottom of header for 3 secs max with heat sink

CELL RESISTANCE VS. ILLUMINANCE



ELECTRO-OPTICAL CHARACTERISTICS TA=25°C (2 HOURS LIGHT ADAPT, MIN)***

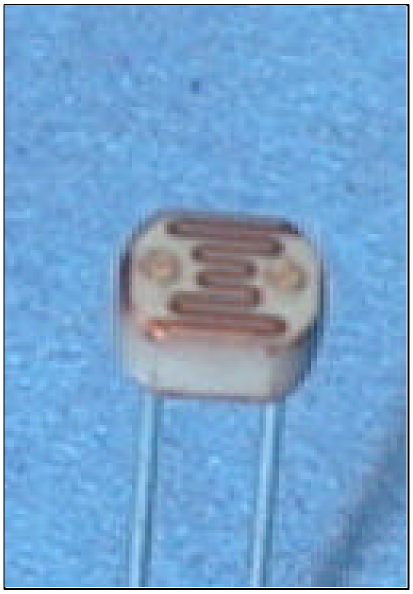
MODEL NO.	CELL RESISTANCE** (Ohms)				SENSITIVITY	SPECTRAL PEAK	RESPONSE TIME @10 Lux	
	10 Lux @2856K		DARK		LOG(R100)-LOG(R10) / LOG (E100)-LOG(E10)	(nm)	RISE TIME (ms)	FALL TIME (ms)
	MIN (KΩ)	MAX (KΩ)	MIN (MΩ)	SEC	(λ TYP)	TYP	TYP	TYP
PDV-P9001	4	11	0.3	10	0.65	520	60	25
PDV-P9002	9	20	0.5	10	0.6	520	60	25
PDV-P9002-1	11	20	0.5	10	0.7	520	60	25
PDV-P9003	16	33	1	10	0.8	520	60	25
PDV-P9003-1	23	33	1	10	0.85	520	60	25
PDV-P9004	27	60	2	10	0.85	520	60	25
PDV-P9005	50	94	2.5	10	0.9	520	60	25
PDV-P9005-1	48	140	20	10	0.9	520	60	25

 **Photocells are light adapted at 100 to 500 Lux. ***Photocells are tested at 2856°K at a 10 Lux light level. Resistance values are for reference only.

[FORM NO. 100-PDV-P9001 REV A]

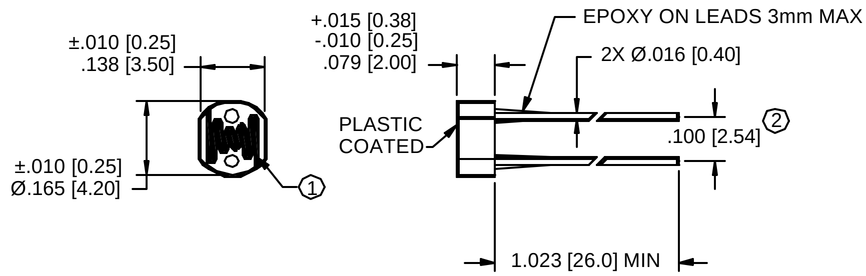
PHOTONIC DETECTORS INC.

Cadmium Sulfoselenide (CdS) Photoconductive Photocells
Type PDV-P9XXX-X



PACKAGE DIMENSIONS INCH [mm]

INDUSTRY EQUIVALENTS: VT900 & NSL5152



PLASTIC COATED CERAMIC PACKAGE

1. PHOTOCELL "GRID" PATTERN CAN VARY, PDI RESERVES THE RIGHT TO CHANGE AND MIX GRID PATTERNS.
2. DIMENSION CONTROLLED AT BASE OF CERAMIC HEADER PACKAGE.

FEATURES

- Visible light response
- Sintered construction
- Low cost
- High Reliability

DESCRIPTION

PDV-P9XXX-X are (CdS) photoconductive photocells designed to sense light from 400 nm to 700 nm. As light dependent resistors, they are available in a wide range of resistance values. They are packaged in a two leaded plastic-coated ceramic header.

APPLICATIONS

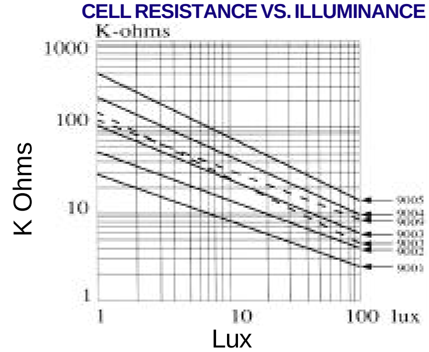
- Camera exposure
- Low light level
- Shutter controls
- Night light controls

ABSOLUTE MAXIMUM RATING (TA=25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{PK}	Applied Voltage		150	V dc
$P_{d\Delta po\Delta t}$	Continuous Power Dissipation		90	mW/°C
T_{stg} & T_o	Operating Temperature Range & Storage	-30	+75	°C
T_S	Soldering Temperature*		+260	°C

*.200 inch (5 mm) from bottom of header for 3 secs max with heat sink

CELL RESISTANCE VS. ILLUMINANCE



ELECTRO-OPTICAL CHARACTERISTICS TA=25°C (2 HOURS LIGHT ADAPT, MIN)***

MODEL NO.	CELL RESISTANCE** (Ohms)				SENSITIVITY	SPECTRAL PEAK	RESPONSE TIME @10 Lux	
	10 Lux @2856K		DARK		LOG(R100)-LOG(R10) / LOG (E100)-LOG(E10)	(nm)	RISE TIME (ms)	FALL TIME (ms)
	MIN (KΩ)	MAX (KΩ)	MIN (MΩ)	SEC	(λ TYP)	TYP	TYP	TYP
PDV-P9006	80	200	5	10	1	520	60	25
PDV-P9007	10	100	1	10	0.8	520	60	25
PDV-P9008	10	200	20	10	0.85	520	60	25
PDV-P9103	20	45	1	10	0.8	520	60	25
PDV-P9200	10	50	5	10	0.9	520	70	15
PDV-P9203	5	20	20	10	0.9	520	70	15

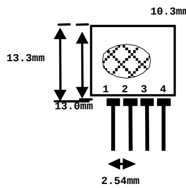
Information in this technical data sheet is believed to be correct and reliable. However, no responsibility is assumed for possible inaccuracies or omission. Specifications are subject to change without notice. ** Photocells are light adapted at 100 to 500 Lux. *** Photocells are tested at 2856°K at a 10 Lux light level. Resistance values are for reference only.

[FORM NO. 100-PDV-P9001 REV A]

TLP434A & RLP434A RF ASK Hybrid Modules for Radio Control (New Version)

Easy-Link Wireless

TLP434A Ultra Small Transmitter



pin 1 : GND
pin 2 : Data In
pin 3 : Vcc
pin 4 : Antenna (RF output)

Frequency 315, 418 and 433.92 Mhz

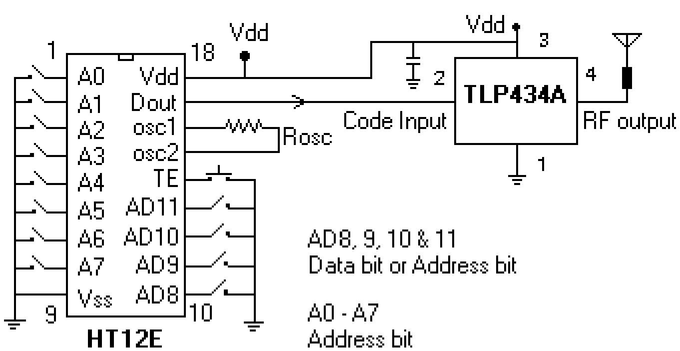
Modulation : ASK
Operation Voltage : 2 - 12 VDC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vcc	Operating supply voltage		2.0	-	12.0	V
Icc 1	Peak Current (2V)		-	-	1.64	mA
Icc 2	Peak Current (12V)		-	-	19.4	mA
Vh	Input High Voltage	Idata= 100uA (High)	Vcc-0.5	Vcc	Vcc+0.5	V
Vl	Input Low Voltage	Idata= 0 uA (Low)	-	-	0.3	V
FO	Absolute Frequency	315Mhz module	314.8	315	315.2	MHz
PO	RF Output Power- 50ohm	Vcc = 9V-12V	-	16	-	dBm
		Vcc = 5V-6V	-	14	-	dBm
DR	Data Rate	External Encoding	512	4.8K	200K	bps

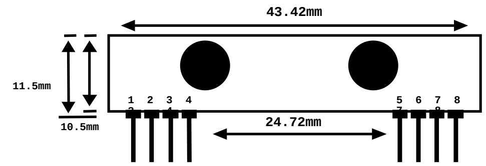
Notes : (Case Temperature = 25°C +- 2°C , Test Load Impedance = 50 ohm)

Application Circuit :

Typical Key-chain Transmitter using HT12E-18DIP, a Binary 12 bit Encoder from Holtek Semiconductor Inc.



RLP434A SAW Based Receiver



pin 1 : Gnd
pin 2 : Digital Data Output
pin 3 : Linear Output /Test
pin 4 : Vcc
pin 5 : Vcc
pin 6 : Gnd
pin 7 : Gnd
pin 8 : Antenna

Frequency 315, 418 and 433.92 Mhz

Modulation : ASK
Supply Voltage : 3.3 - 6.0 VDC
Output : Digital & Linear

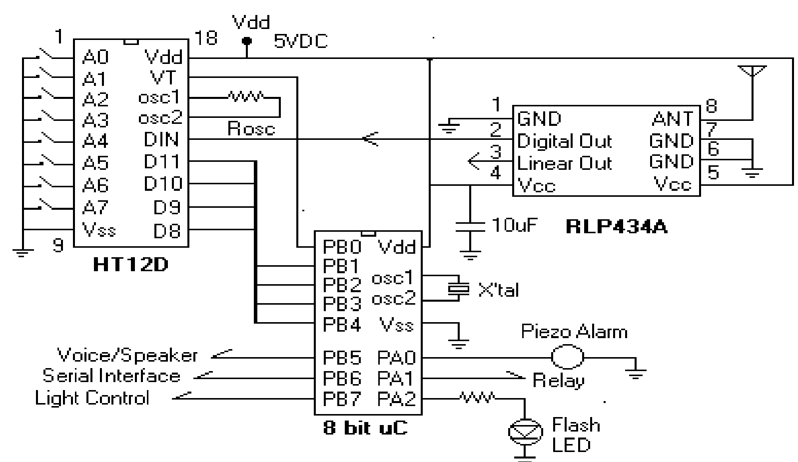
Symbol	Parameter	Conditions	Min	Typ	Max	
Vcc	Operating supply voltage		3.3	5.0V	6.0	V
Itot	Operating Current		-	4.5		mA
Vdata	Data Out	Idata = +200 uA (High)	Vcc-0.5	-	Vcc	V
		Idata = -10 uA (Low)	-	-	0.3	V

Electrical Characteristics

Characteristics	SYM	Min	Typ	Max	Unit
Operation Radio Frequency	FC	315, 418 and 433.92			MHz
Sensitivity	Pref		-110		dBm
Channel Width			+-500		Khz
Noise Equivalent BW			4		Khz
Receiver Turn On Time			5		ms
Operation Temperature	Top	-20	-	80	C
Baseboard Data Rate			4.8		KHz

Application Circuit :

Typical RF Receiver using HT12D-18DIP, a Binary 12 bit Decoder with 8 bit uC HT48RXX from Holtek Semiconductor Inc.



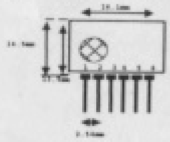
Laipac Technology, Inc.
105 West Beaver Creek Rd. Unit 207 Richmond Hill Ontario L4B 1C6 Canada
Tel: (905)762-1228 Fax: (905)763-1737 e-mail: info@laipac.com

LAIPAC TECH

TLP/RLP434 RF ASK Low Cost Hybrid Modules for Radio Control and Telemetry applications

Easy-Link Wireless

TLP-434 Transmitter



pin 1 : Vcc
pin 2 : Vcc
pin 3 : Gnd
pin 4 : Gnd
pin 5 : RF Output
pin 6 : Digital Data Input

Frequency 315, 418 and 433.92MHz

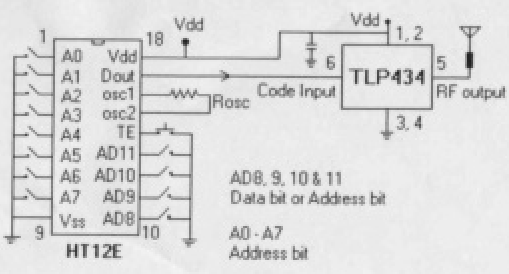
Modulation : ASK
Operation Voltage : 2 - 12 VDC
RF Output Power : 8mW @3.6V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vcc	Operating supply voltage		2.0	-	12.0	V
Icc	Peak Current		-	5	-	mA
Vh	Input High Voltage	Idata= 100uA (High)	Vcc-0.5	Vcc	Vcc+0.5	V
Vl	Input Low Voltage	Idata= 0 uA (Low)	-	-	0.3	V
FO	Absolute Frequency	315Mhz module	314.8	315	315.2	MHz
	Relative To 433.92MHz			+/-150	+/-200	KHz
PO	RF Output Power- 50ohm	Vcc = 9V to 12V	-	16	-	dBm
		Vcc = 5V to 6V	-	14	-	dBm
DR	Data Rate	External Encoding	-	2.4K	3K	bps

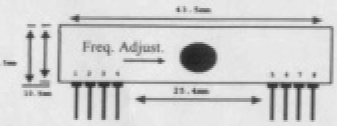
Notes : (Case Temperature = 25°C +- 2°C , Test Load Impedance = 50 ohm)

Application Circuit I:

Typical Key-chain Transmitter using HT12E-18DIP, a Binary 12 bit Encoder from Holtek Semiconductor Inc.



RLP-434 Receiver



pin 1 : Gnd
pin 2 : Digital Data Output
pin 3 : Linear Output
pin 4 : Vcc
pin 5 : Vcc
pin 6 : Gnd
pin 7 : Gnd
pin 8 : Antenna (About 30 - 35 cm)

Frequency 315, 418 and 433.92MHz

Modulation : ASK
Supply Voltage : 4.5 - 5.5 VDC
Output : Digital & Linear
Sensitivity : 3uVrms

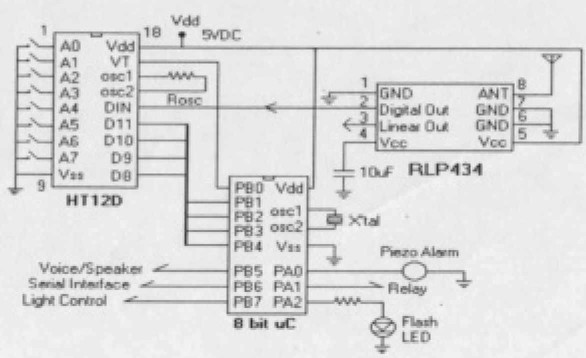
Symbol	Parameter	Conditions	Min	Typ	Max	
Vcc	Operating supply voltage		4.5	5	5.5	V
Itot	Operating Current		-	3.5	4.5	mA
Vdata	Data Out	Idata = +200 uA (High)	Vcc-0.5	-	Vcc	V
		Idata = -10 uA (Low)	-	-	0.3	V

Electrical Characteristics

Characteristics	SYM	Min	Typ	Max	Unit
Operation Radio Frequency	FC		315, 418 and 434		MHz
Sensitivity	Pref	-100	-103	-106	dBm
Channel Width			+-1.5		Khz
Receiver Turn On Time			5		ms
Noise equivalent BW	NEB		4		Khz
Baseboard Data Rate			3	5	Khz

Application Circuit II:

Typical RF Receiver using HT12D-18DIP, a Binary 12 bit Decoder with 8 bit uC HT48RXX from Holtek Semiconductor Inc.



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LAIPAC TECH

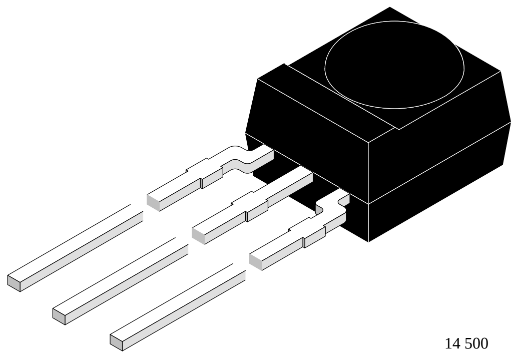
Photo Modules for PCM Remote Control Systems

Available types for different carrier frequencies

Type	fo	Type	fo
TSOP1830	30 kHz	TSOP1833	33 kHz
TSOP1836	36 kHz	TSOP1837	36.7 kHz
TSOP1838	38 kHz	TSOP1840	40 kHz
TSOP1856	56 kHz		

Description

The TSOP18.. – series are miniaturized receivers for infrared remote control systems. PIN diode and preamplifier are assembled on lead frame, the epoxy package is designed as IR filter.
The demodulated output signal can directly be decoded by a microprocessor. The main benefit is the reliable function even in disturbed ambient and the protection against uncontrolled output pulses.



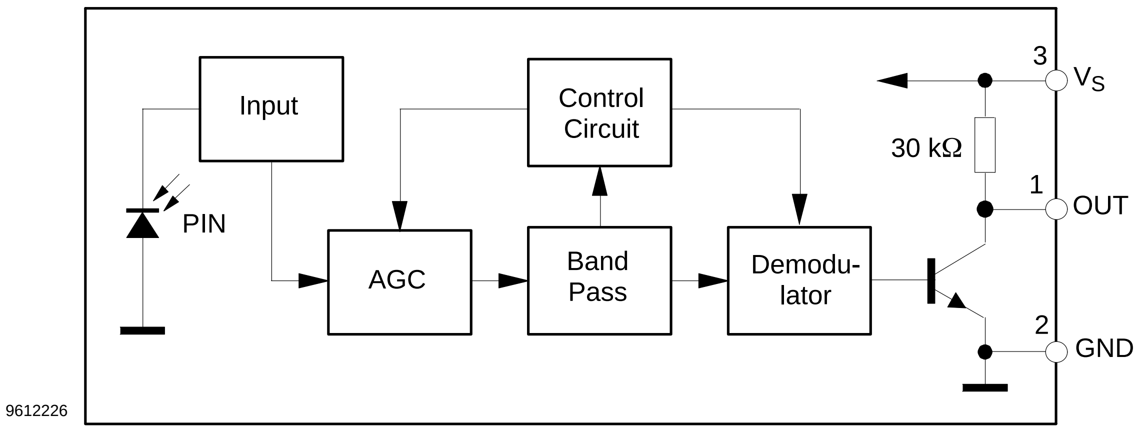
Features

- Photo detector and preamplifier in one package
- Internal filter for PCM frequency
- TTL and CMOS compatibility
- Output active low
- Improved shielding against electrical field disturbance
- Suitable burst length ≥6 cycles/burst

Special Features

- Small size package
- Enhanced immunity against all kinds of disturbance light
- No occurrence of disturbance pulses at the output
- Short settling time after power on (<200μs)

Block Diagram



Absolute Maximum Ratings

T_{amb} = 25°C

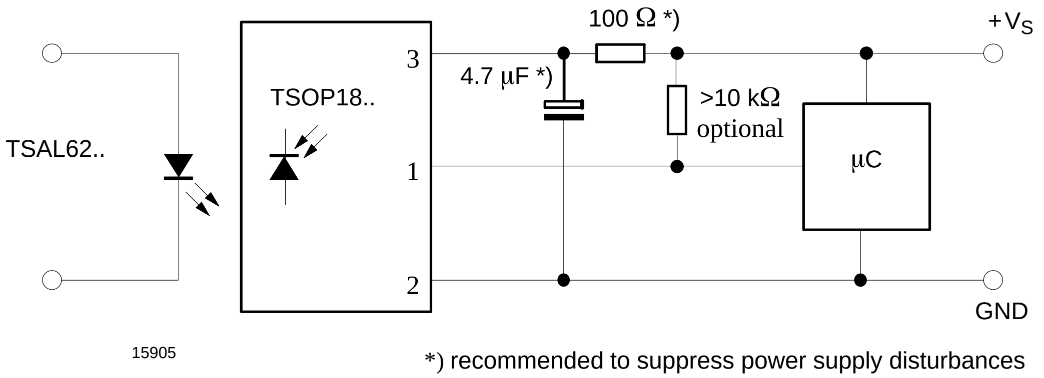
Parameter	Test Conditions	Symbol	Value	Unit
Supply Voltage	(Pin 3)	V_S	–0.3...6.0	V
Supply Current	(Pin 3)	I_S	5	mA
Output Voltage	(Pin 1)	V_O	–0.3...6.0	V
Output Current	(Pin 1)	I_O	5	mA
Junction Temperature		T_j	100	°C
Storage Temperature Range		T_{stg}	–25...+85	°C
Operating Temperature Range		T_{amb}	–25...+85	°C
Power Consumption	(T_{amb} ≦ 85 °C)	P_{tot}	50	mW
Soldering Temperature	t ≦ 10 s, 1 mm from case	T_{sd}	260	°C

Basic Characteristics

T_{amb} = 25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Supply Current (Pin 3)	V_S = 5 V, E_v = 0	I_{SD}	0.9	1.2	1.5	mA
	V_S = 5 V, E_v = 40 klx, sunlight	I_{SH}		1.3		
Supply Voltage (Pin 3)		V_S	4.5		5.5	V
Transmission Distance	E_v = 0, test signal see fig.6, IR diode TSAL6200, I_F = 300 mA	d		35		m
Output Voltage Low (Pin 1)	I_{OSL} = 0.5 mA,E_e = 0.7 mW/m^2, f = f_o	V_{OSL}			250	mV
Irradiance (30 – 40 kHz)	Pulse width tolerance: $t_{pi} - 4/f_o < t_{po} < t_{pi} + 6/f_o$, test signal see fig.6	$E_{e\ min}$		0.3	0.5	mW/m^2
Irradiance (56 kHz)				0.4	0.7	
Irradiance		$E_{e\ max}$	30			W/m^2
Directivity	Angle of half transmission distance	$\varphi_{1/2}$		±45		deg

Application Circuit



*) recommended to suppress power supply disturbances

Suitable Data Format

The circuit of the TSOP18.. is designed in that way that unexpected output pulses due to noise or disturbance signals are avoided. A bandpassfilter, an integrator stage and an automatic gain control are used to suppress such disturbances.
The distinguishing mark between data signal (not suppressed) and disturbance signal (supressed) are carrier frequency, burst length and Signal Gap Time (see diagram below).

The data signal should fullfill the following condition:

- Carrier frequency should be close to center frequency of the bandpass (e.g. 38kHz).
- Burst length should be 6 cycles/burst or longer.
- After each burst a gap time of at least 9 cycles is neccessary.
- The data format should not make a continuous signal transmission. There must be a Signal Gap Time (longer than 15ms) at least each 90ms (see Figure A).

Some examples for suitable data format are: NEC Code (repetitive pulse), NEC Code (repetitive data), Toshiba Micom Format, Sharp Code, RC5 Code, RECS–80 Code, R–2000 Code.

When a disturbance signal is applied to the TSOP18.. it can still receive the data signal. However the sensitivity is reduced to that level that no unexpected pulses will occure.

Some examples for such disturbance signals which are suppressed by the TSOP18.. are:

- DC light (e.g. from tungsten bulb or sunlight),
- Continuous signal at 38kHz or at any other frequency,
- Signals from fluorescent lamps (see Figure B).
- Continuous IR signal (e.g. 1ms burst, 2ms pause)

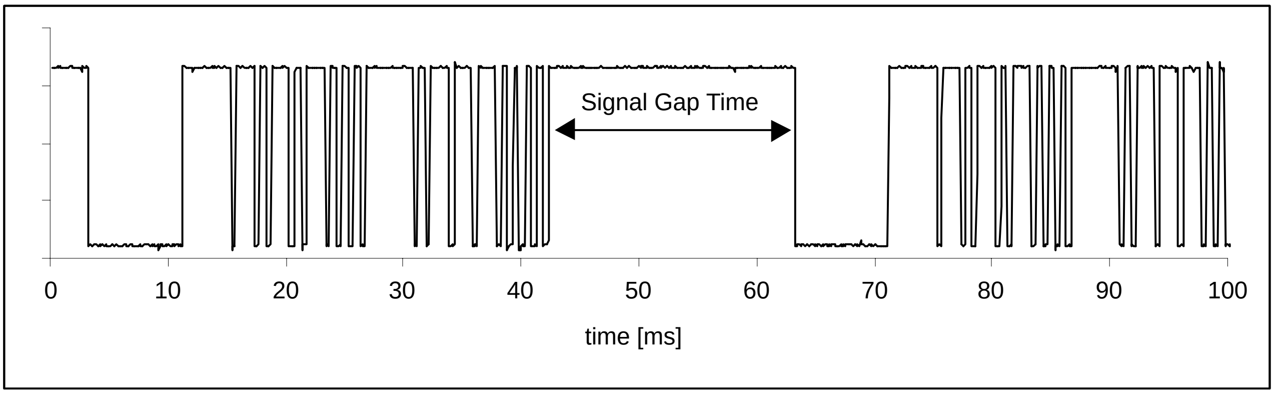


Figure A: Data Signal (Output of IR Receiver) with a Signal Gap Time of 20ms

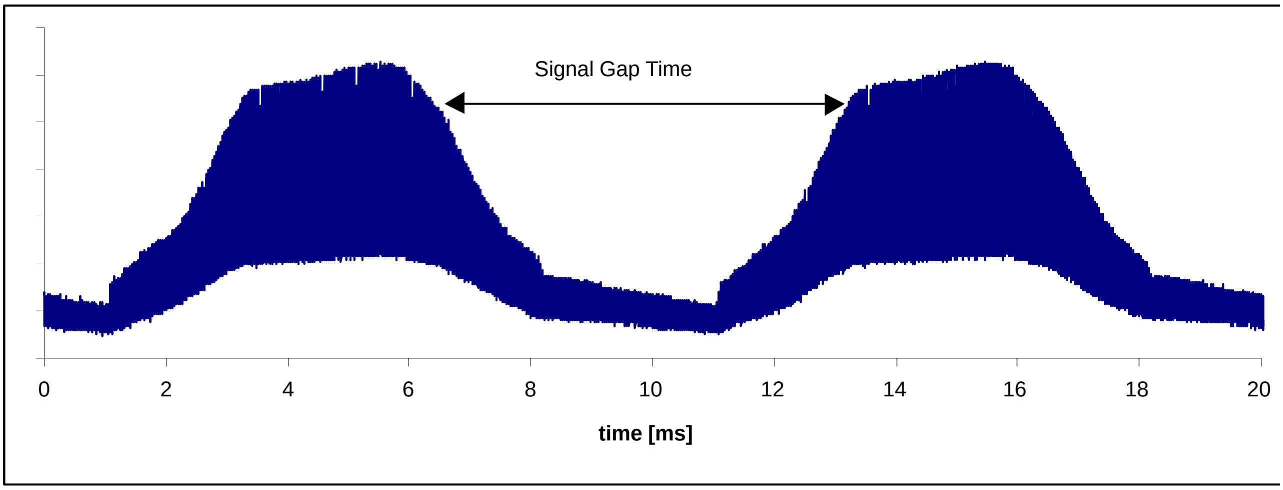


Figure B: Disturbance Signal from Fluorescent Lamp with Signal Gap Time of 7ms

Typical Characteristics (T_{amb} = 25°C unless otherwise specified)

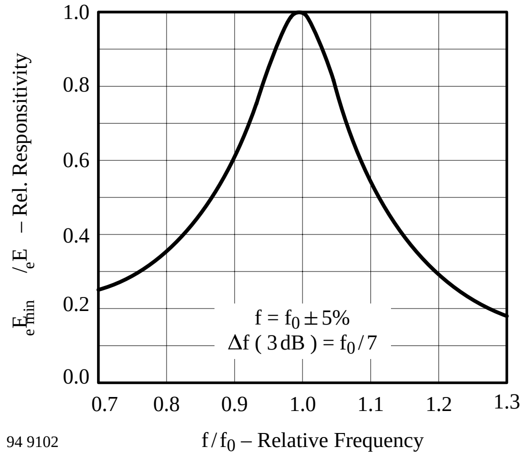


Figure 1. Frequency Dependence of Responsivity

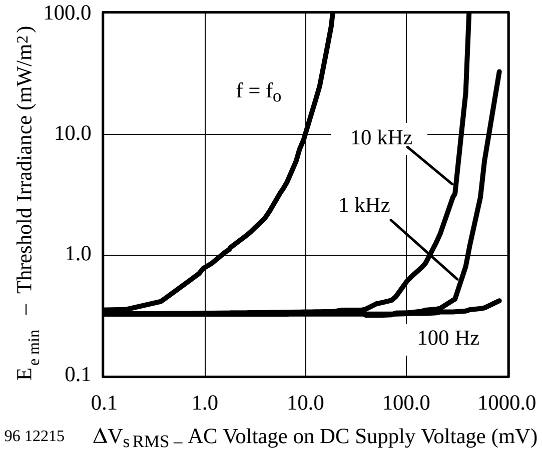


Figure 4. Sensitivity vs. Supply Voltage Disturbances

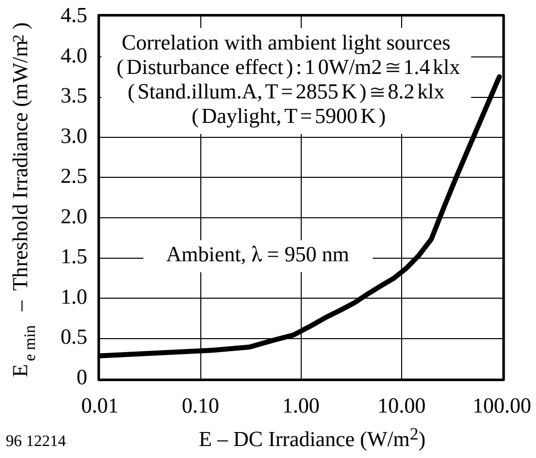


Figure 2. Sensitivity in Bright Ambient

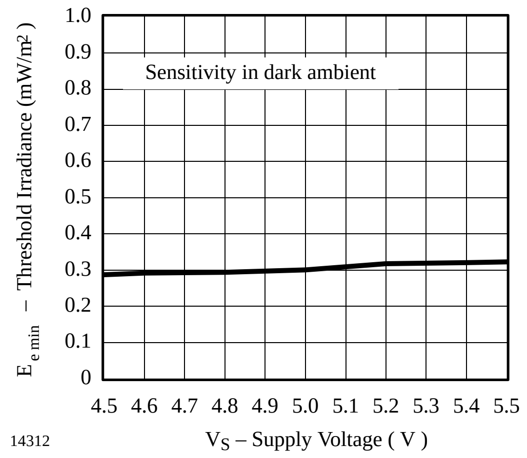


Figure 5. Sensitivity vs. Supply Voltage

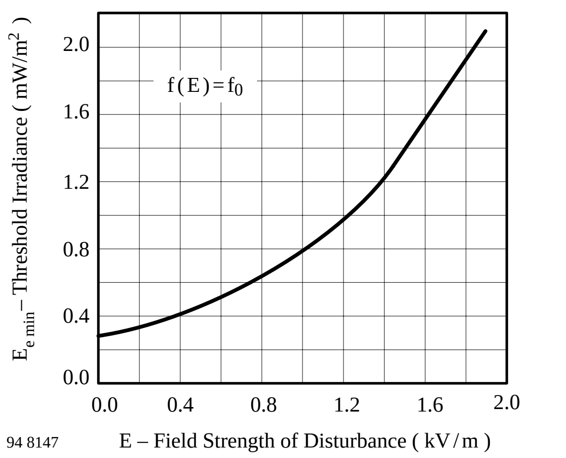


Figure 3. Sensitivity vs. Electric Field Disturbances

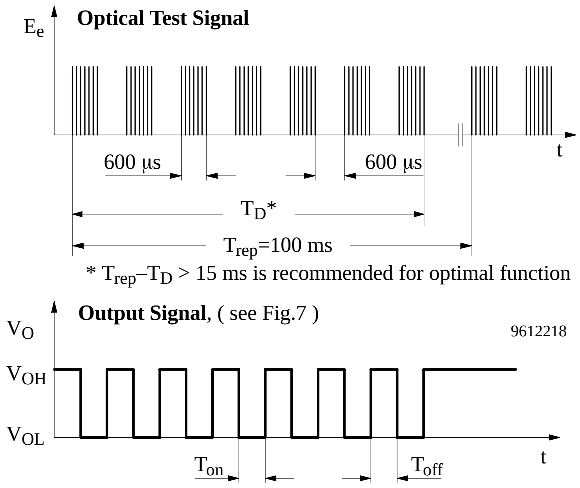


Figure 6. Output Function

Document Number 82047
Rev. 13, 13-Sep-00

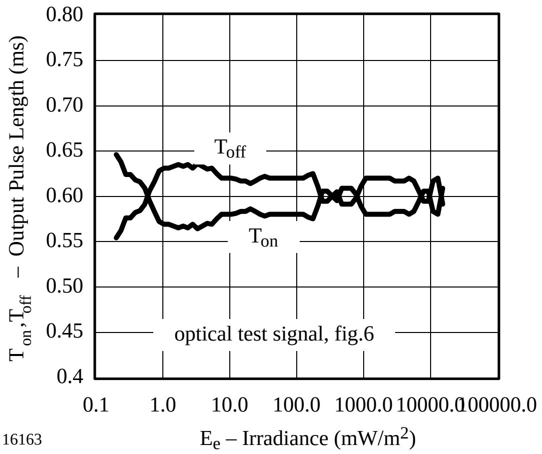


Figure 7.

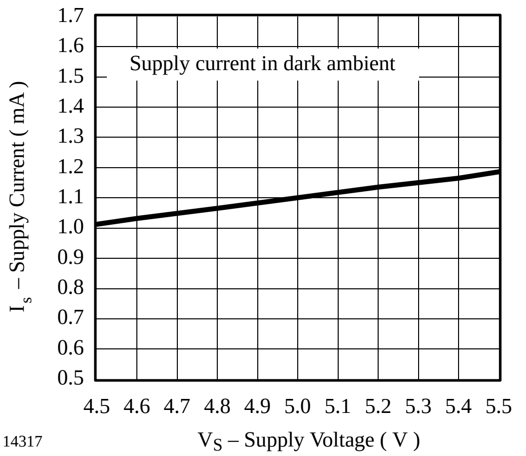


Figure 10. Supply Current vs. Supply Voltage

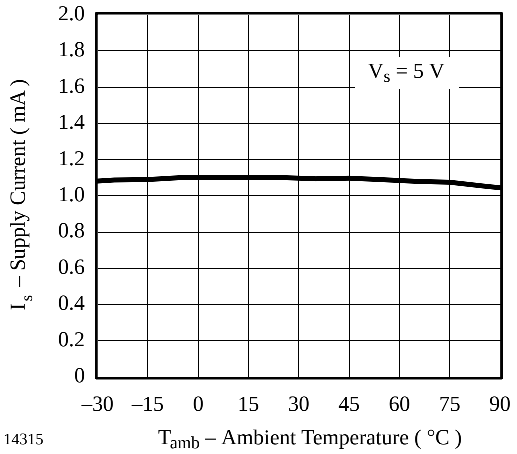


Figure 8. Supply Current vs. Ambient Temperature

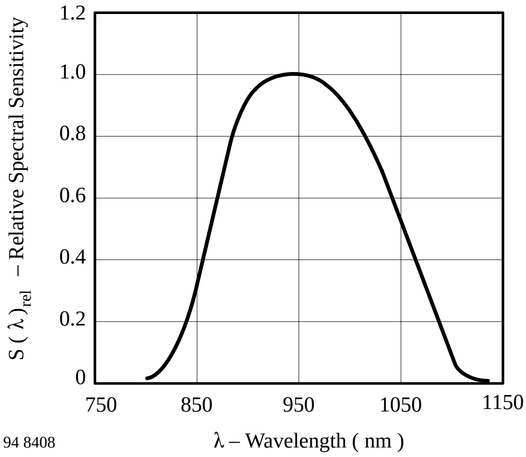


Figure 11. Relative Spectral Sensitivity vs. Wavelength

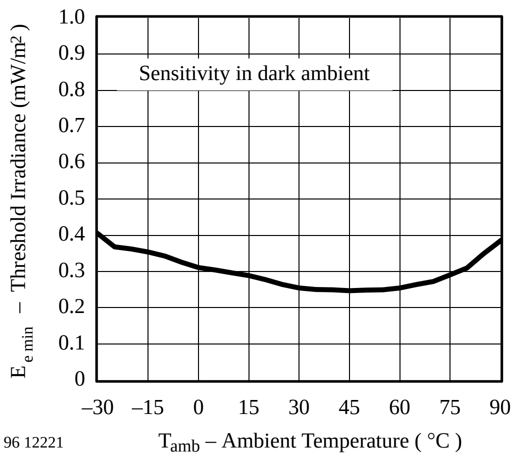


Figure 9. Sensitivity vs. Ambient Temperature

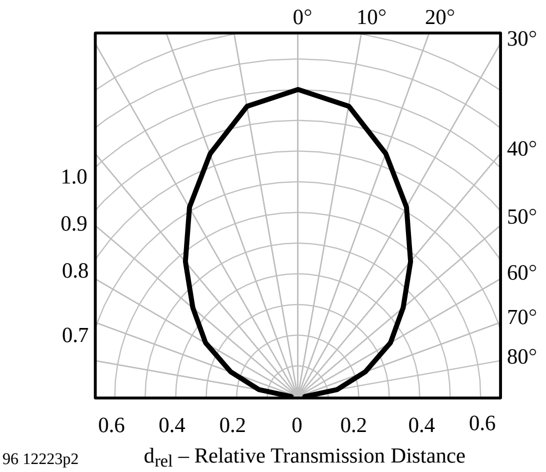
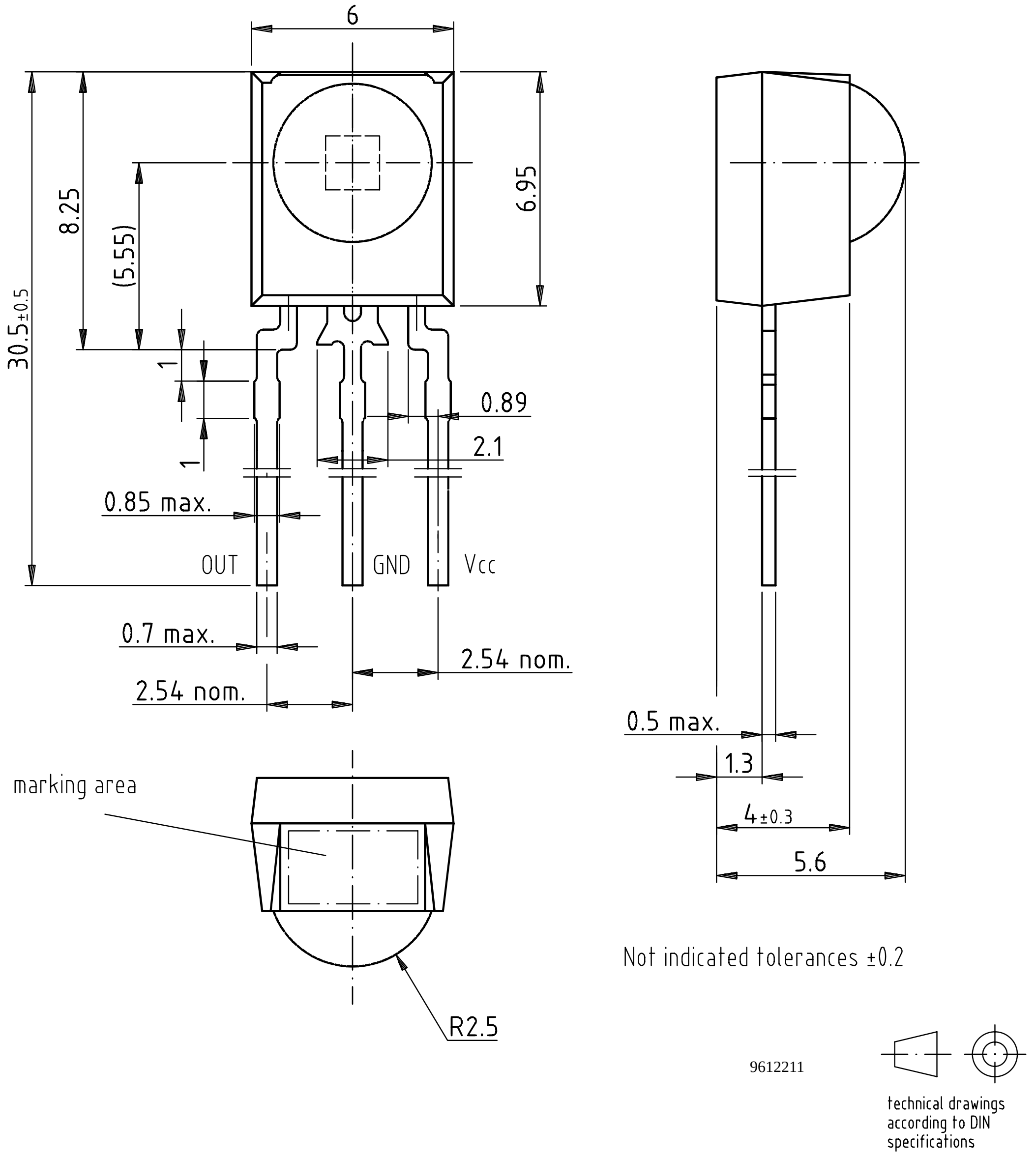


Figure 12. Directivity

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423

GP2Y0A02YK

Long Distance Measuring Sensor

■ Features

1. Less influence on the colors of reflected objects and their reflectivity, due to optical triangle measuring method
2. Distance output type
   (Detection range:20 to 150cm)
3. An external control circuit is not necessary
   Output can be connected directly to a microcomputer

■ Applications

1. For detection of human body and various types of objects in home appliances, OA equipment, etc

■ Absolute Maximum Ratings

(T_a=25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.3 to +7	V
*1 Output terminal voltage	V_O	-0.3 to V_{CC} +0.3	V
Operating temperature	T_{opr}	-10 to +60	°C
Storage temperature	T_{stg}	-40 to +70	°C

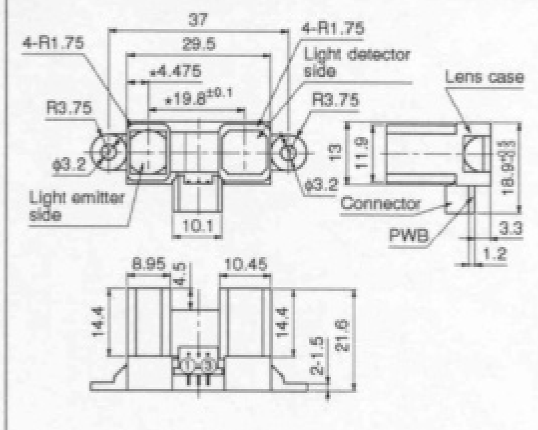
*1 Open collector output

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Operating Supply voltage	V_{CC}	4.5 to 5.5	V

■ Outline Dimensions

(Unit : mm)



Terminal connection
① V_O
② GND
③ V_{CC}

* The dimensions marked * are described the dimensions of lens center position.
* Unspecified tolerance : ±0.3mm

■ Electro-optical Characteristics

(T_a=25°C, V_{CC}=5V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Distance measuring range	ΔL	*2 *3	20	–	150	cm
Output terminal voltage	V_O	*2 L=150cm	0.25	0.4	0.55	V
Difference of output voltage	ΔV_O	*2 Output change at L=150cm to 20cm	1.8	2.05	2.3	V
Average dissipation current	I_{CC}	–	–	33	50	mA

Note) L:Distance to reflective object
*2 Using reflective object:White paper (Made by Kodak Co. Ltd. gray cards R-27 · white face, reflective ratio;90%)
*3 Distance measuring range of the optical sensor system

Fig.1 Internal Block Diagram

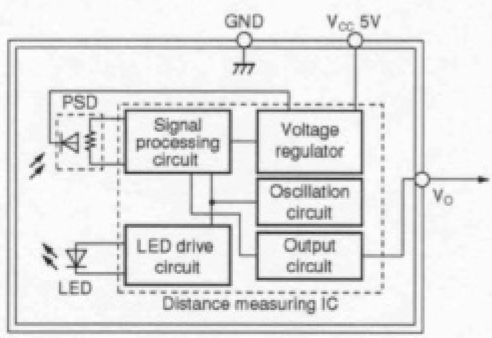


Fig.2 Timing Chart

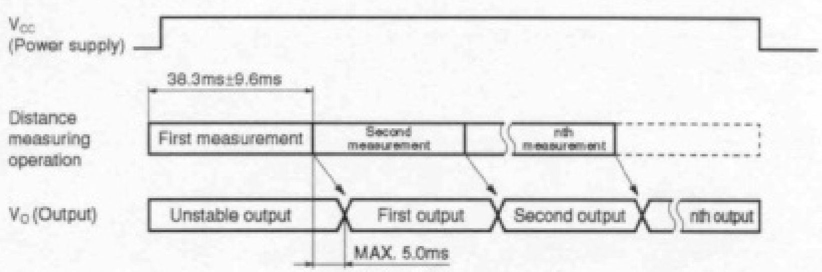
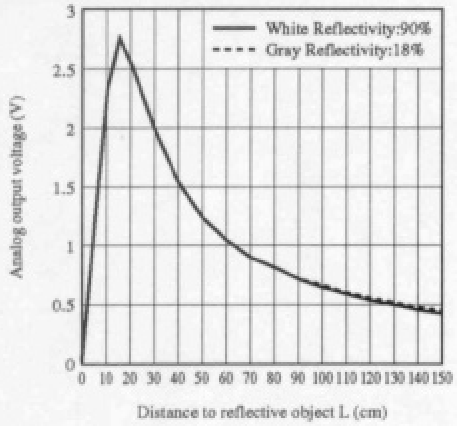


Fig.3 Analog Output Voltage vs. Distance to Reflective Object



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- Observe the following points when using any devices in this publication. SHARP takes no responsibility for damage caused by improper use of the devices which does not meet the conditions and absolute maximum ratings to be used specified in the relevant specification sheet nor meet the following conditions:

  (i) The devices in this publication are designed for use in general electronic equipment designs such as:
  --- Personal computers
  --- Office automation equipment
  --- Telecommunication equipment [terminal]
  --- Test and measurement equipment
  --- Industrial control
  --- Audio visual equipment
  --- Consumer electronics

  (ii) Measures such as fail-safe function and redundant design should be taken to ensure reliability and safety when SHARP devices are used for or in connection with equipment that requires higher reliability such as:
  --- Transportation control and safety equipment (i.e., aircraft, trains, automobiles, etc.)
  --- Traffic signals
  --- Gas leakage sensor breakers
  --- Alarm equipment
  --- Various safety devices, etc.

  (iii) SHARP devices shall not be used for or in connection with equipment that requires an extremely high level of reliability and safety such as:
  --- Space applications
  --- Telecommunication equipment [trunk lines]
  --- Nuclear power control equipment
  --- Medical and other life support equipment (e.g., scuba).

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